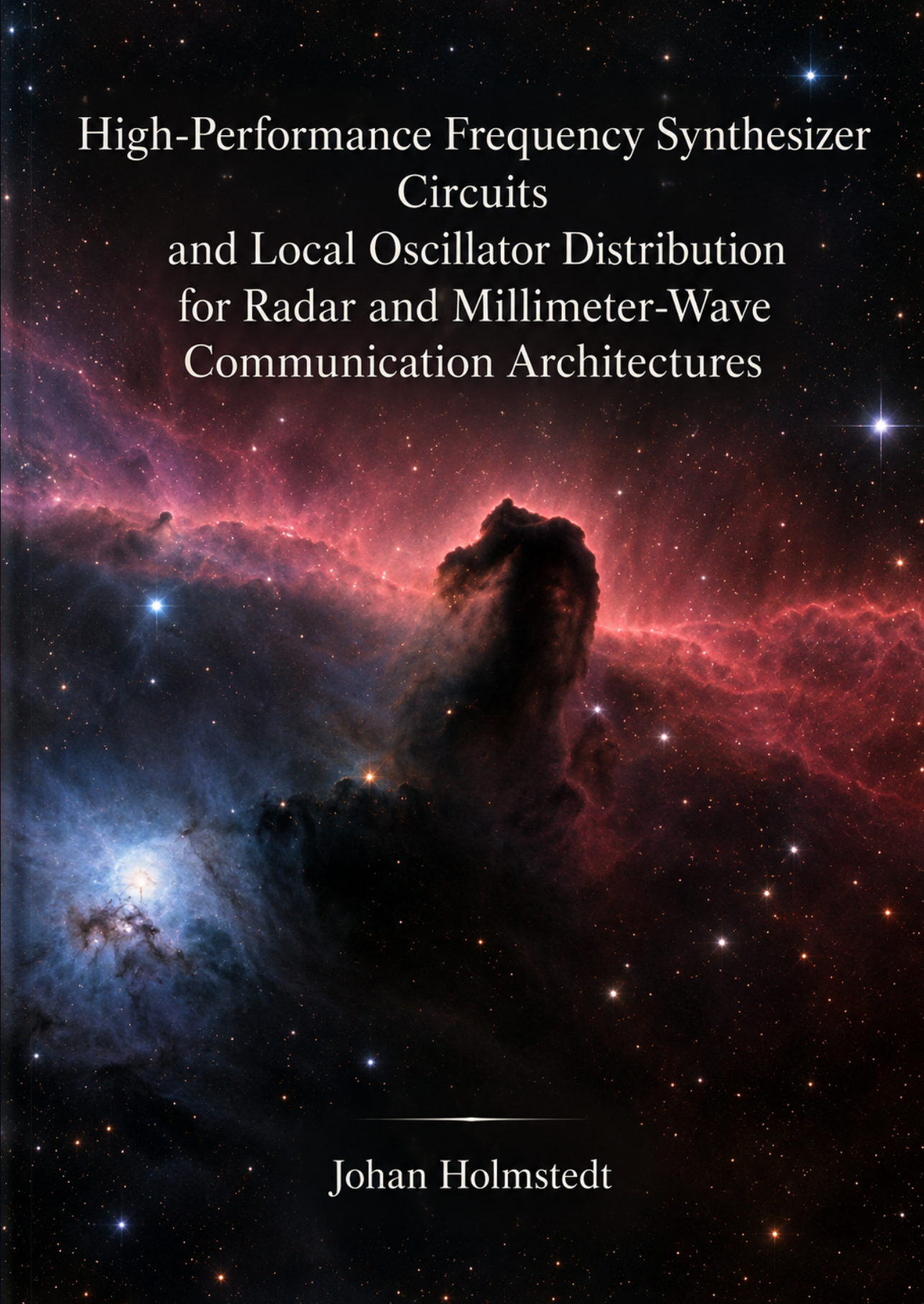
High-Performance Frequency Synthesizer Circuits and Local Oscillator Distribution for Radar and Millimeter-Wave Communication Architectures



Johan Holmstedt

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High-Performance Frequency Synthesizer Circuits and Local Oscillator Distribution for Radar and Millimeter-Wave Communication Architectures

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr. S.K. Lenaerts, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op dinsdag 8 december 2026 om 16:00 uur

door

Carl Johan Viktor Holmstedt

geboren te Lund, Zweden

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Summary

Title: High-Performance Frequency Synthesizer Circuits and Local Oscillator Distribution for Radar and Millimeter-Wave Communication Architectures

This work addresses key challenges in oscillator signal generation and distribution for millimeter-wave (mmWave) communication and radar systems. To enable further improvements in overall system performance, several critical issues must be considered. These include the development of power-efficient local oscillator (LO) distribution architectures and ultra-low phase-noise fractional-N phase-locked loops (PLLs) for next-generation FR2 transceivers and Wi-Fi systems. In addition, frequency-modulated continuous-wave (FMCW) radar systems with high dynamic range require highly linear frequency chirps and extremely low phase noise. Furthermore, in FMCW multiple-input multiple-output (MIMO) radar systems, correlation of phase noise between the transmitter (TX) and receiver (RX) is essential to suppress phase-noise spillover from TX to RX. All these aspects must be carefully addressed while maintaining low power consumption.

The work carried out has resulted in the following research contributions:

- An improved frequency doubler is proposed by incorporating a PMOS pair into a conventional push–pull full-wave rectified doubler. This modification enhances drain efficiency through current reuse and enables a larger output swing. Importantly, it allows the use of a differential-to-differential transformer with a higher quality factor, thereby avoiding losses caused by poor balancing. The proposed doubler is implemented in 28-nm bulk CMOS to validate the concept.
- A pseudo-differential digital-to-time converter (DTC) is proposed. It improves linearity by suppressing even-order distortions and offers additional benefits such as improved supply sensitivity rejection. Furthermore, high performance can be achieved with simpler digital calibration. An N-fractional PLL is implemented in 28-nm bulk CMOS to demonstrate the proposed approach.
- A theoretical study is conducted on the effects of linearity and quantization noise when multiple sigma–delta modulators operate in parallel with time offsets

in an N-fractional PLL. Explicit closed-form expressions for fractional spur suppression are derived and verified through simulations.

- A theoretical investigation of systematic distortions in FMCW radar chirps is presented. The resulting analysis provides new insights and leads to an improved methodology for benchmarking chirp linearity.

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List of symbols and abbreviations

Symbol	Description	Unit
BER	Bit error rate	
CP	Charge pump	
CPE	Common phase error	
DNL	Differential non-linearity	LSB
DPLL	Digital phase-locked loop	
DTC	Digital-to-time converter	
EM	Electromagnetic	
ENOB	Effective number of bits	bit
ICI	Inter-carrier interference	
IF	Intermediate frequency	
ILFM	Injection-locked frequency multiplier	
INL	Integral non-linearity	LSB
LNA	Low-noise amplifier	
LO	Local oscillator	
LRR	Long-range radar	
MASH	Multi-stage noise shaping	
NF	Noise figure	dB
PA	Power amplifier	
PAE	Power-added efficiency	%
PFD	Phase-frequency detector	
PNN	Periodic nonlinearity noise	
PVT	Process, voltage, and temperature	
QN	Quantization noise	
RCS	Radar cross-section	m^2
RF	Radio frequency	
RMS	Root mean square	
SDM	Sigma–delta modulator	
SFDR	Spurious-free dynamic range	dB
SNDR	Signal-to-noise-and-distortion ratio	dB
SPD	Sampling phase detector	
SRR	Short-range radar	
TDC	Time-to-digital converter	
THD	Total harmonic distortion	dB
ULA	Uniform linear array	
UWB	Ultra-wideband	

Symbol	Description	Unit
VCO	Voltage-controlled oscillator	
A_{NL2}	Maximum second-order nonlinear time deviation	s
A_{NL3}	Maximum third-order nonlinear time deviation	s
f_c	Carrier frequency	Hz
f_L	Injection-locking range	Hz
f_u	OFDM subcarrier spacing	Hz
G_r	Receive antenna gain	
G_t	Transmit antenna gain	
P_r	Received power	W
P_t	Transmitted power	W
T_{chirp}	Chirp duration	s
T_{frame}	Frame duration	s
T_{ref}	Reference clock period	s
T_{VCO}	VCO oscillation period	s
ΔR	Range resolution	m
$\Delta\theta$	Angular resolution	rad
Δv	Velocity resolution	m/s
λ	Wavelength	m
σ_ϕ	RMS phase jitter	rad
σ_t	RMS time jitter	s
τ	Time delay	s

Chapter 1

Introduction

1.1 Background

Historically, wireless communication systems have primarily operated in the sub-6 GHz frequency bands. This preference is due to several advantages, including favorable link budgets, longer channel coherence times, easier signal generation, and more efficient power amplification, among others. These characteristics make sub-6 GHz frequencies well suited for reliable wide-area coverage.

However, in high-density urban environments, the sub-6 GHz spectrum is no longer sufficient to meet the rapidly increasing demand for wireless data traffic [1]. The limited available bandwidth in these lower frequency bands leads to network congestion and reduced system performance. Consequently, modern wireless communication systems have increasingly moved toward higher carrier frequencies.

To address these limitations, contemporary wireless standards such as 5G increasingly utilize millimeter-wave (mmWave) frequency bands, where substantially larger bandwidths are available. In this context, FR2 (Radio Frequency 2) technologies play a crucial role by enabling significantly higher data throughput, lower latency, and improved spectral efficiency.

A similar trend can be observed in sensing systems, particularly in automotive radar. Current developments in advanced driver-assistance systems (ADAS) and the gradual transition toward autonomous driving are driving increasingly stringent requirements on radar performance. As a result, the legacy 24 GHz automotive radar band is rapidly being replaced by the 77 GHz band, where substantially larger bandwidths are available. The increased bandwidth enables improved range resolution, while the shorter wavelength at higher frequencies allows a larger number of transmit (TX) and receive (RX) antennas to be integrated within the same physical aperture, thereby improving angular resolution.

Furthermore, the growing interest in joint communication and sensing (JCAS) systems further motivates the convergence of communication and radar platforms toward higher carrier frequencies, since both domains benefit from large available bandwidths and compact antenna integration.

However, operation at substantially higher frequencies also introduces several important challenges. These include increased path loss, difficulties in generating sufficient output power, degraded phase-noise performance, more stringent requirements on RF signal generation and distribution circuitry, and worse receiver sensitivity, making it harder to meet the link budget. These challenges are particularly critical in mmWave and sub-THz systems, where the performance of frequency generation and chirp synthesis circuits often becomes a key system-level bottleneck.

1.2 Problem statement

While significant research has been conducted on FR2 5G circuits, several challenges remain unresolved. In this work, the focus is placed on local oscillator (LO) generation and distribution. In FR2 5G systems, the use of higher-order modulation schemes, such as 256-QAM, imposes stringent requirements on phase noise and integrated jitter [2]. This is particularly critical when a large portion of the EVM budget is allocated to the power amplifier, thereby placing even tighter constraints on the LO performance. These requirements call for efficient and well-designed LO generation and distribution architectures. For example, the phase-locked loop (PLL) may be implemented at a lower frequency, followed by distribution and subsequent upconversion closer to the RF front-end, in order to optimize performance and mitigate loss and noise degradation.

It is plausible that future automotive radar systems will migrate toward the D-band (110–170 GHz), as these frequencies offer significantly larger available bandwidth, reduced spectral congestion, and lower interference. This enables improved range resolution as well as enhanced angular resolution. Additionally, the shorter wavelength at higher frequencies allows more transmit (TX) and receive (RX) elements to be integrated within the same physical aperture, which is particularly important in aperture-limited systems, as increasing the number of TX and RX elements further enhances angular resolution. However, transitioning from 77 GHz to D-band frequencies introduces substantial challenges. Phase noise becomes more pronounced, and careful LO planning is essential to ensure sufficient LO power, proper phase synchronization, and suppression of TX–RX leakage. Furthermore, in frequency-modulated continuous-wave (FMCW) radar systems, LO generation is closely tied to chirp generation, which must exhibit extremely high linearity to achieve the dynamic range required for high-performance radar operation.

1.3 Original contributions

The key ideas and original research contributions of this work are summarized as follows:

- A new and, in the author's opinion, improved benchmarking methodology is proposed for linear frequency chirps in the context of FMCW radar systems. This method more accurately captures radar system performance compared to currently prevailing benchmarking approaches. In addition to conventional time-domain analysis, the proposed methodology evaluates frequency deviations in the frequency domain, providing a more comprehensive assessment of chirp linearity.

- An improved frequency doubler is proposed by adding a PMOS pair to the conventional push–pull full-wave rectified doubler. This modification provides higher drain efficiency through current reuse and enables a larger output swing. Most importantly, it allows the use of a differential-to-differential transformer, which has a higher quality factor and avoids losses caused by poor balancing. A D-band doubler is implemented in 28-nm bulk CMOS to demonstrate the proposed concept.

- To the best of the author's knowledge, this is the first work to derive closed-form, simple expressions for the relationship between fractional-N PLL loop nonlinearity and the resulting fractional spurs.

- A theoretical study of the effects on linearity and quantization noise when several sigma–delta modulators are operated in parallel with time offsets in the context of an N-fractional PLL is conducted. Explicit closed-form expressions for the suppression of fractional spurs are derived and verified using simulations.

- A pseudo-differential DTC is proposed. It improves linearity by suppressing even-order distortions. Additionally, it provides several other benefits, such as improved supply sensitivity rejection and better performance can be achieved with simpler digital calibration. An N-fractional PLL is implemented in 28-nm bulk CMOS to demonstrate the proposed concept.

1.4 Outline of the thesis

- **Chapter 2** discusses the error vector magnitude (EVM) requirements for 5G FR2 millimeter-wave systems. An illustrative EVM budget incorporating phase noise contributions is presented, highlighting the impact of local oscillator (LO) generation and distribution on EVM degradation. Both common phase errors and inter-carrier phase errors are analyzed in detail. Furthermore, LO generation architectures are briefly discussed, along with their implications for overall system performance.

- **Chapter 3** provides an overview of frequency allocations for commercial radar systems, followed by a brief introduction to the basic operating principles of frequency-modulated continuous-wave (FMCW) radars. The feasibility of utilizing the D-band for automotive radar applications is also discussed, highlighting associated challenges and opportunities. Furthermore, an analytical approach is used to analyze chirp linearity. Closed-form expressions are derived, and key insights are illustrated through representative examples. Based on these insights, improved benchmarking methodologies for chirp linearity are proposed. In addition, dynamic range requirements are analyzed to highlight the importance of chirp linearity. Finally, a brief discussion on local oscillator (LO) distribution architectures and their impact on FMCW radar performance is presented.
- **Chapter 4** presents the design and analysis of frequency multipliers, with particular emphasis on injection-locked frequency multipliers and harmonic multiplier architectures. The proposed frequency multiplier is implemented in 28 nm CMOS bulk technology. Its operating principles are described in detail, followed by a comprehensive evaluation based on measurement results. The advantages and limitations of the proposed design are also discussed.
- **Chapter 5** discuss the trade-offs between various PLL architectures are discussed. Simple Closed-form analytical expressions are derived to characterize the relationship between fractional-N PLL loop nonlinearity and the resulting fractional spurs. Furthermore, the operation of multiple sigma-delta modulators driven out of phase within a fractional-N PLL is analyzed, and explicit expressions describing their behavior are presented. Several new insights are derived from the analysis. In addition, a differential digital-to-time converter (DTC) architecture is proposed. The implementation of the PLL in 28 nm CMOS technology is described in detail.
- **Chapter 6** presents the conclusions are drawn and recommendations for future research are presented.

Chapter 2

System-Level Considerations for Local Oscillator Generation and Distribution for Millimeter-Wave Communication

In this chapter, the requirements for 5G FR2 millimeter-wave systems are discussed. Particular emphasis is placed on the local oscillator and its phase noise requirements for different modulation schemes.

2.1 5G NR FR2 Requirements

The 5G NR (New Radio) standard is issued by the 3rd Generation Partnership Project (3GPP) and defines the allowed operating frequency bands, transmission schemes, and performance requirements for 5G systems. Within the 5G NR framework, the millimeter-wave (mmWave) bands particularly in the Frequency Range 2 (FR2) spectrum have attracted considerable attention due to the abundance of unused bandwidth available for high-capacity applications.

Different regions have allocated specific millimeter-wave (mmWave) bands for 5G use [3]. For example, in the United States, the 26.5–29.5 GHz (n257), 27.5–28.35 GHz (n261), 37–40 GHz (n260), and 47.2–48.2 GHz (n262) bands are designated; in Europe, the 24.25–27.5 GHz (n258) band is prominent; and other regions have their own mmWave allocations depending on regulatory approval.

In the downlink (DL) direction, 5G NR supports high-order modulation schemes using cyclic prefix orthogonal frequency-division multiplexing (CP-OFDM). The standard includes modulation formats such as QPSK, 16-QAM, 64-QAM, and 256-QAM [4], which are essential for achieving high spectral efficiency under varying channel conditions.

According to the latest 3GPP release [5], the standard specifies strict limits on Error Vector Magnitude (EVM) a critical measure of signal quality for each modulation type. These EVM limits are summarized in Table 2.1, which lists the maximum allowable EVM values for QPSK, 16-QAM, 64-QAM, and 256-QAM. These limits ensure that the transmitted and received signals meet the required quality thresholds to support reliable high-speed communication.

Table 2.1: Summary of EVM Limits (per 3GPP TS 38.104)

Modulation	**EVM Limit (%)**	**EVM Limit (dB)**
QPSK	17.5%	–15.14 dB
16-QAM	12.5%	–18.06 dB
64-QAM	8.0%	–21.94 dB
256-QAM	3.5%	–29.12 dB

In a practical transceiver chain, several hardware impairments contribute to the overall Error Vector Magnitude (EVM). Below, some critical error sources are summarized.

- **Power Amplifier (PA) Nonlinearities**: Cause constellation compression as well as AM/AM and AM/PM distortion, especially near saturation. This is often the hardest effect to fully linearize and is a major contributor to the overall EVM budget.
- **Thermal Noise Receiver NF (noise figure) and LNA (low-noise amplifier) Contribution**: Adds a random noise floor, which becomes dominant

at low signal powers or near the receiver's sensitivity limit. The receiver's overall NF, largely determined by the performance of the LNA, sets the effective thermal noise floor of the system.

- **Sampling Jitter, ADC/DAC Nonlinearity, and Quantization Noise**: Sampling jitter from DAC and ADC clocks effectively converts to phase noise, particularly critical at millimeter-wave frequencies or when using high-speed data converters. In addition to clock stability, the inherent nonlinearity of the ADC and DAC components, as well as their quantization noise, contribute directly to the overall EVM. These impairments must be carefully balanced through calibration and system design.
- **Phase Noise (PLL, LO, VCO)**: Adds phase jitter, leading to common phase error (CPE) and inter-carrier interference (ICI). This effect is especially critical in OFDM-based systems and when using high-order QAM, where constellation points are tightly packed.
- **IQ Imbalance (Mixers, DACs, ADCs)**: Produces quadrature errors, image distortion, image rejection ratio and LO leakage.

In most practical systems, the majority of the EVM budget is allocated to the power amplifier [6], as it presents a poor linearity-to-efficiency trade-off, especially when driven near its compression region. Secondly, the next largest contributor is often the analog-to-digital converter (ADC) [7], as the intermediate frequency (IF) bandwidth is relatively high, and designing high-frequency, high-resolution (many-bit) ADCs becomes increasingly challenging and power-hungry. As the system bandwidth increases, ADC performance becomes more critical, requiring a fair share of the EVM budget to maintain overall system performance [7].

This leaves only a smaller portion of the EVM budget for phase noise and spurious tones from the phase-locked loop (PLL) and system synthesizer. Adding to the challenge, high-frequency reference crystals can be both power-hungry and costly in monetary terms, effectively ruling them out for low-cost, high-volume applications such as handsets, and thus complicating the design further [2].

2.2 5G NR FR2 Phase Noise Requirements

Phase noise affects signal constellations differently depending on its frequency components. For very low-frequency phase noise, the entire constellation diagram undergoes a rotation, introducing what is known as common phase error (CPE). This type of impairment is typically addressed using pilot-based correction schemes [8] or clock recovery techniques.

The variance of the CPE can be calculated by applying a weighting function to the phase noise power spectral density, as given in Equation 2.1, where $S_\phi(f)$ is the phase noise power spectral density and $f_u = 1/T_{\text{sym}}$ is the subcarrier spacing, determined

by the useful symbol duration of the OFDM system [9].

$$\sigma^2_{\mathrm{CPE}} = \int_{-\infty}^{\infty} S_\phi(f) \operatorname{sinc}^2\left(\frac{f}{f_u}\right) df \tag{2.1}$$

The higher-frequency components of phase noise — specifically those with frequencies larger than f_u contribute to inter-carrier interference (ICI). In this case, phase noise causes the energy of each subcarrier to spread into adjacent subcarriers, effectively rotating individual constellation points relative to one another. This results in constellation distortion, degraded error vector magnitude (EVM), and ultimately increased bit error rates (BER). The total variance contributed by the ICI is calculated using Equation 2.2, [9].

$$\sigma^2_{\mathrm{ICI}} = \int_{-\infty}^{\infty} S_\phi(f) \left[1 - \operatorname{sinc}^2\left(\frac{f}{f_u}\right)\right] df \tag{2.2}$$

The connection between error vector magnitude (EVM) and phase noise is given by Equation 2.3, where the integrated single-sided phase noise (in dBc) is related to the overall root-mean-square (RMS) phase jitter.

$$\mathrm{EVM}_{\mathrm{rms}} \approx \sigma_\phi \tag{2.3}$$

Furthermore, using Equations 2.3 and 2.4, one can estimate the phase noise requirements for local oscillator (LO) generation under different modulation schemes. Specifically, Equation 2.4 relates the RMS time jitter σ_t to the RMS phase jitter σ_ϕ at the carrier frequency f_c.

$$\sigma_t = \frac{\sigma_\phi}{2\pi f_c} \tag{2.4}$$

Notably, Equation 2.4 illustrates the well-known fact that phase noise requirements become increasingly stringent as the carrier frequency increases.

Table 2.2 summarizes the time jitter requirements for systems operating at 28 GHz (the lower end of the FR2 band) and 47 GHz (the upper end of the FR2 band) across different modulation schemes. The table compares two cases: (1) where the synthesizer is allocated 100% of the EVM budget and (2) where only 10% of the EVM budget is allocated to the synthesizer generation, in order to give a bigger noise and distortion budget to other blocks. From these results, it becomes clear that meeting phase noise requirements at higher frequencies poses significant challenges to the capabilities of state-of-the-art phase-locked loops (PLLs).

Further complicating the matter, LO generation often needs to support N-fractional operation, as modern communication systems frequently employ complex carrier aggregation schemes [2].

Table 2.2: EVM and Corresponding Time Jitter Requirements at 28 GHz and 47 GHz

Modulation	EVM (%)	28 GHz	47 GHz	28 GHz (10%)	47 GHz (10%)
QPSK	17.5	995 fs	592 fs	99.5 fs	59.2 fs
16-QAM	12.5	710 fs	423 fs	71.0 fs	42.3 fs
64-QAM	8.0	455 fs	271 fs	45.5 fs	27.1 fs
256-QAM	3.5	199 fs	119 fs	19.9 fs	11.9 fs

2.3 Local oscillator distribution architecture

The first question concerning the system design of phased-array and MIMO communication systems with respect to oscillator generation and distribution, is whether a single PLLs or multiple PLLs should be employed.

In millimeter-wave (mmWave) communication systems, RF beamforming is often used due to the high power consumption of digital beamforming with large baseband bandwidths. In this case, signal distribution is performed in the RF domain.

In MIMO systems, employing more than one PLL can reduce the overall power consumption of the system. This is because the reference crystal signal can be distributed instead of the RF oscillator signal. Since the crystal reference signal operates at a frequency that is at least an order of magnitude lower, the power required for its distribution is substantially reduced. Furthermore, in MIMO systems, the PLL performance requirements are relaxed when multiple PLLs are used, provided that their phase noise is uncorrelated.

A drawback of employing more than one PLL on the same chip is the potential coupling between oscillators. Such coupling can lead to degraded system performance and, in the worst case, oscillation instability [10], [11].

The high requirements placed on phase-locked loops (PLLs) make direct implementation at RF frequencies impractical, as high-frequency PLLs suffer from both poor phase noise performance and degraded figure of merit (FOM) [2].

One possible solution is to use a heterodyne receiver, as illustrated in Fig, 2.1 (a). This approach allows the PLL output frequency to be lowered, and I/Q generation can be relatively easily achieved using a quadrature divider. However, the image signal must be carefully addressed, [12]. Additionally, mixers tend to contribute higher noise, which must be considered. An alternative implementation is to apply a frequency multiplier, as shown in Fig, 2.1 (b). This homodyne receiver architecture allows for direct IF image elimination, mitigating the image issue entirely. However, this approach requires I/Q generation at RF frequencies, which can potentially degrade performance due to increased I/Q mismatch.

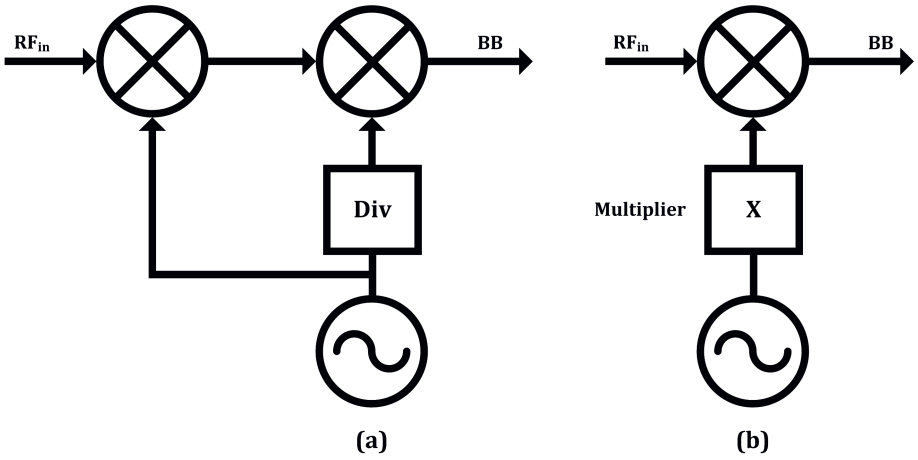


Figure 2.1: Schematics of: (a) Heterodyne receiver (b) Homodyne receiver employing a frequency multiplier.

Chapter 3

System-Level Consideration for Local Oscillator Generation and Distribution for Radar

This chapter provides a brief introduction to FMCW radar concepts, including range resolution, angular resolution, and velocity estimation. The challenges and potential advantages of D-band radar systems are also discussed. Furthermore, the commonly used benchmarking methodology for linear frequency chirps is revisited, and an alternative benchmarking approach with improved correlation to actual radar-system performance is proposed. Finally, the chapter concludes with a discussion of local-oscillator (LO) distribution architectures for mmWave FMCW radar systems.

3.1 Introduction

Table 3.1 outlines the key millimeter-wave radar frequency bands used in industrial, presence detection, and smart home applications. These systems typically rely on continuous-wave radar—most notably Frequency-Modulated Continuous-Wave (FMCW) radar—due to its low power consumption and ability to provide both range and velocity information. Compared to pulsed radar, FMCW offers simpler hardware implementation and is well-suited to the short- to mid-range requirements of industrial and automotive use cases.

3.1.1 Industrial and Smart Sensing Applications

The 24.00–24.25 GHz ISM band is widely used in legacy systems for motion sensing, automatic doors, and basic proximity detection. While the narrow 250 MHz bandwidth limits range resolution, it remains popular due to global availability and mature ecosystem support. The 60 GHz band (57.00–64.00 GHz) provides a significantly wider 7 GHz bandwidth and is increasingly used in smart home and IoT applications such as gesture recognition and people counting. Its unlicensed status and overlap with 802.11ad make it convenient for consumer-grade integration.

The 122.00–123.00 GHz band, while more niche, offers opportunities for high-resolution short-range sensing in industrial environments. Its high frequency results in stronger atmospheric attenuation, which, while limiting range, also reduces interference—making it well-suited for environments with high device density.

3.1.2 Automotive Radar Spectrum Evolution

FMCW radar plays a dominant role in the automotive sector due to its ability to simultaneously provide range, velocity, and angle-of-arrival information with high precision and low power. As shown in Table 3.1, the automotive radar spectrum has evolved significantly over time to support increasingly complex driver-assistance and autonomous driving features.

The 24.00–24.25 GHz band was traditionally used for short-range radar (SRR) in blind-spot monitoring and parking assistance. However, this band is being phased out in many regions due to congestion and regulatory shifts. The 21.65–26.65 GHz UWB allocation, used primarily in Europe, provided a wider bandwidth for improved resolution but remains geographically limited in adoption.

Modern automotive radar systems are rapidly transitioning to the 76–81 GHz range. The 76.00–77.00 GHz band is globally recognized for long-range radar (LRR), essential for adaptive cruise control and highway safety applications. More recently, the 77.00–81.00 GHz band has become the standard for universal radar coverage—enabling short-, mid-, and long-range detection with up to 4 GHz of bandwidth. This allows for higher resolution, MIMO capability, and better interference mitigation, making it ideal for advanced driver-assistance systems (ADAS) and full autonomous navigation.

Overall, the evolution of radar bands reflects the growing demand for high-resolution sensing across both industrial and automotive sectors, with FMCW radar serving as the technology backbone due to its scalability, accuracy, and efficiency.

Table 3.1: Millimeter-Wave Radar Bands for Industrial and Automotive Applications

Application	**Frequency Band (GHz)**	**Band width**	**Explanation**
Industrial / Presence Detection / Smart Home	24.00–24.25	250 MHz	Unlicensed ISM band; used for motion sensing, automatic doors, and basic proximity detection. Limited resolution due to narrow bandwidth.
	57.00–64.00	7 GHz	License-free ISM band in US/EU; widely used for gesture recognition, people counting, and smart home/IoT sensing. Also shared with Wi-Fi (802.11ad).
	122.00–123.00	1 GHz	Short-range high-frequency band for industrial sensing (e.g., liquid level monitoring, collision avoidance). Low interference due to atmospheric attenuation.
Automotive Radar	24.00–24.25	250 MHz	Legacy short-range radar (SRR); still deployed in blind-spot detection and parking assist. Being phased out in favor of higher bands.
	21.65–26.65	Up to 5 GHz	UWB band allocated in Europe for automotive SRR. Wide bandwidth allows improved range resolution but limited to specific regions.
	76.00–77.00	1 GHz	Globally allocated for long-range radar (LRR), e.g., adaptive cruise control. Narrower bandwidth than newer bands.
	77.00–81.00	4 GHz	Modern universal automotive radar band for short-, mid-, and long-range radar. Enables MIMO, fine resolution, and high target separation. Increasing global adoption.

3.2 FMCW Basic Operational Principles

Figure 3.1 illustrates a highly simplified FMCW radar transceiver block diagram. The transmit (Tx) signal is generated by the chirp generation block and transmitted toward the target. A time-delayed and attenuated version of the signal is reflected back to the receiver antenna and mixed with the transmitted signal. After low-pass filtering, only the intermediate frequency (IF) remains, which is proportional to the target's distance.

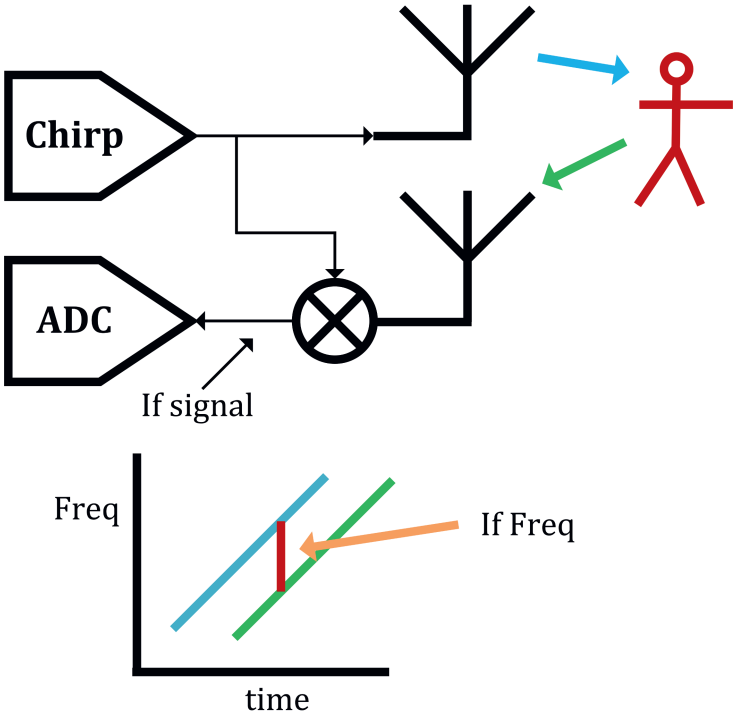


Figure 3.1: Simplified figure of an FMCW radar transceiver.

3.2.1 Range Resolution

Range resolution ΔR determines the minimum distinguishable distance between two closely spaced objects and is primarily determined by the chirp bandwidth B:

$$\Delta R = \frac{c}{2B} \tag{3.1}$$

where c is the speed of light (in meters per second, m/s), and B is the chirp bandwidth (in hertz, Hz). The resulting range resolution ΔR is expressed in meters (m) [13].

3.2.2 Velocity (Doppler) Resolution and Ambiguity

In FMCW radar, multiple chirps are transmitted in a frame to resolve velocity using phase shifts between successive chirps. The velocity resolution Δv depends on the total duration of the chirp frame $T_{\text{frame}} = NT_{\text{chirp}}$, where N is the number of chirps:

$$\Delta v = \frac{\lambda}{2T_{\text{frame}}} = \frac{\lambda}{2NT_{\text{chirp}}} \tag{3.2}$$

where λ is the radar wavelength (in meters, m), T_{frame} is the total duration of the chirp frame (in seconds, s), T_{chirp} is the duration of a single chirp (in seconds, s), and N is a dimensionless count of chirps. The resulting velocity resolution Δv is expressed in meters per second (m/s).

The maximum unambiguous velocity v_{max} is limited by the chirp repetition interval T_{chirp}:

$$v_{\text{max}} = \frac{\lambda}{4T_{\text{chirp}}} \tag{3.3}$$

Thus, there is a trade-off: longer T_{chirp} increases velocity resolution but reduces unambiguous velocity [13].

3.2.3 Angular Resolution

Angular resolution refers to the radar's ability to distinguish between two targets located at different angles. In MIMO (Multiple Input Multiple Output) radar systems, multiple transmit and receive antennas are used to synthesize a virtual antenna array with more elements and a larger effective aperture than the physical antenna arrays alone, thereby improving angular resolution [13].

The maximum number of virtual elements is given by

$$N_v = N_{\text{TX}} N_{\text{RX}}, \tag{3.4}$$

where:

- N_{TX} is the number of transmit antennas,
- N_{RX} is the number of receive antennas.

However, obtaining $N_{\text{TX}} N_{\text{RX}}$ unique virtual elements requires a carefully designed antenna geometry. The virtual element positions are determined by the sums of the transmit and receive antenna positions. Only when these positions form a uniformly spaced arrangement can the virtual array be modeled as a Uniform Linear Array (ULA).

Assuming the MIMO radar synthesizes a virtual ULA with inter-element spacing d (m), the angular resolution $\Delta\theta$ (rad) is approximately determined by the virtual array aperture:

$$\Delta\theta \approx \frac{\lambda}{2D}, \tag{3.5}$$

where D is the effective aperture of the virtual array. For a virtual ULA with approximately $N_{\mathrm{TX}}N_{\mathrm{RX}}$ uniformly spaced virtual elements,

$$D \approx (N_{\mathrm{TX}}N_{\mathrm{RX}} - 1)d, \tag{3.6}$$

giving

$$\Delta\theta \approx \frac{\lambda}{2(N_{\mathrm{TX}}N_{\mathrm{RX}} - 1)d}. \tag{3.7}$$

For sufficiently large arrays, this is often approximated as

$$\Delta\theta \approx \frac{\lambda}{2N_{\mathrm{TX}}N_{\mathrm{RX}}d}. \tag{3.8}$$

This expression shows that increasing either the number of virtual elements or the effective aperture improves angular resolution. To avoid spatial aliasing (grating lobes), the virtual inter-element spacing is typically chosen such that

$$d \leq \frac{\lambda}{2}. \tag{3.9}$$

Note: The assumption here is that the MIMO radar synthesizes a virtual ULA.

3.3 Motivation for D-Band in Automotive Radar

The D-band (110–170 GHz) has emerged as a strong candidate for next-generation automotive radar systems. This interest stems from several compelling advantages over currently deployed radar frequency bands (e.g., 24 GHz, 60 GHz, and 76–81 GHz). Below, we discuss the motivations in detail, with reference to radar system design parameters and practical constraints in automotive applications.

3.3.1 Benefits of D-Band

1. Increased Bandwidth and Range Resolution:
The D-band offers significantly more available bandwidth than existing automotive

radar bands. Since range resolution ΔR is inversely proportional to bandwidth B, as shown in Equation 3.1, a larger bandwidth enables better range resolution. This is particularly beneficial for near-field imaging and detailed object separation in dense environments.

2. Improved Angular Resolution with Smaller Apertures:
Angular resolution depends on both the wavelength λ, the physical aperture size D, and the number of transmit (Tx) and receive (Rx) antenna elements. It is approximately given by Equation 3.8. Since D-band wavelengths are roughly half those in the 76–81 GHz band, equivalent angular resolution can be achieved with proportionally smaller apertures. In addition, more Tx and Rx antenna elements can be accommodated within the same physical aperture, enabling higher angular sampling and improved spatial resolution.

This is particularly attractive in automotive radar design, where manufacturers often prioritize aesthetics and impose strict constraints on the size and placement of external sensors.

Moreover, angular resolution is often the limiting factor in practical radar system performance. For example, [14] reports an angular resolution of only 30 degrees, while the range resolution is already within a few centimeters. Therefore, improving angular resolution is a key motivation for exploring higher frequency bands such as D-band.

3. Spectrum Availability and Interference Mitigation:
D-band is relatively underutilized and offers significantly more spectrum compared to legacy radar bands. This not only allows for higher resolution but also for improved coexistence: more systems can operate simultaneously with less interference, as use are spread out over more bandwidth. Additionally, the poor propagation properties at D-band (i.e., higher atmospheric attenuation) inherently limit the radar range, which can be beneficial in dense environments by reducing cross-interference between users.

4. Opportunities for Clean-Slate Regulation:
Radar spectrum and standards are currently relatively unregulated. There are no widely adopted specifications for how different radar systems should coordinate or share bandwidth to minimize mutual interference. If such regulatory frameworks were introduced in existing radar bands (e.g., 24 GHz or 76–81 GHz), they would need to coexist with a wide variety of legacy systems using different modulation schemes and waveform formats.

In contrast, the D-band presents a unique regulatory opportunity: it offers a relatively unused portion of the spectrum, free from legacy radar deployments. This opens the door for a harmonized, radar-specific allocation that could support advanced features such as dynamic interference mitigation, waveform standardization, and spectrum sharing protocols across manufacturers. By starting with a clean slate, regulators and industry stakeholders could collaboratively define future-ready rules optimized

specifically for high-resolution radar sensing.

Unfortunately, however, radar waveform design and interference mitigation strategies are often considered proprietary features and competitive differentiators among automotive radar manufacturers. This complicates the regulatory process, as manufacturers may be reluctant to adopt standardized solutions that reduce product differentiation.

3.3.2 Reasons to Not Explore D-Band for Automotive Radar

While D-band presents many advantages, it also introduces or exacerbates several challenges:

1. Power Amplifier Efficiency and Output Power:
At D-band, power amplifiers exhibit lower power-added efficiency (PAE) and reduced output power. This issue is particularly severe in silicon-based technologies, as the D-band lies near or beyond half of the maximum frequency ($f_{\max}$) achievable in scaled silicon processes. As a result, the available output power is limited, which directly constrains the achievable radar range.

2. Increased Phase Noise Sensitivity:
Phase noise tends to worsen at higher carrier frequencies. Since phase noise can limit radar dynamic range in certain scenarios, it may become a critical impairment at D-band.

3. Lower Velocity Ambiguity Limit:
The maximum unambiguous velocity $v_{\max}$ in FMCW systems is inversely related to the chirp repetition interval, Equation 3.3. This makes high-speed target tracking more challenging without careful waveform design. Additionally, faster chirps place stricter requirements on the linearity and accuracy of the chirp frequency deviation.

4. Limited Propagation Range: D-band signals suffer greater free-space path loss and atmospheric absorption. While this reduces interference, it also limits operational range—making D-band radar more suitable for short-range applications such as parking assist, low-speed maneuvering, or object imaging.

3.3.3 Summary

Advantages:

- **Increased bandwidth** → finer range resolution.
- **Shorter wavelength** → better angular resolution for a given aperture.
- **Greater spectrum** → reduced interference and room for more simultaneous radar users.

- **Regulatory opportunities** → potential for radar-optimized spectrum management.

Disadvantages:

- **Lower power amplifier efficiency** and reduced output power.
- **Worsened phase noise** performance at higher frequencies.
- **Reduced velocity ambiguity** for high-speed objects.
- **Limited propagation range**, constraining long-distance applications.

In conclusion, D-band radar holds significant potential for future automotive systems, particularly in high-resolution, short-range applications. However, realizing this potential requires overcoming significant hardware and regulatory challenges. Early adoption may be driven by use cases that demand fine angular and range resolution, such as in-cabin monitoring, parking automation, or pedestrian imaging.

3.4 Radar Equation and Dynamic Range Considerations

The fundamental radar equation describes the received power P_r from a target at distance R as:

$$P_r = \frac{P_t \, G_t \, G_r \, \lambda^2 \, \sigma}{(4\pi)^3 R^4} \tag{3.10}$$

where:

- P_r — Received power [W]
- P_t — Transmitted power [W]
- G_t — Transmit antenna gain [unitless (ratio)]
- G_r — Receive antenna gain [unitless (ratio)]
- λ — Wavelength of the transmitted signal [m]
- σ — Radar cross-section (RCS) of the target [m^2]
- R — Distance to the target [m]

The R^4 dependence in the denominator of the radar equation is particularly important, as it implies that the received power decreases rapidly with increasing target distance. Specifically, a target at 100 m produces a received signal that is 80 dB weaker than the same target at 1 m, assuming constant radar cross section (RCS).

This severe attenuation imposes stringent dynamic range requirements on the radar receiver.

Moreover, the RCS itself varies significantly between different objects. As summarized in Table 3.2, a truck may exhibit an RCS as high as 30 dBsm, whereas a small child may have an RCS as low as −5 dBsm. Consequently, the received power difference between a nearby truck, for example at 4 m, and a distant child, for example at 30 m, can exceed 80 dB. In automotive radar applications, where reliable detection of vulnerable road users is safety-critical, the weakest expected target return must remain sufficiently above the noise floor, typically by at least 20–30 dB, depending on the required probability of detection and false-alarm rate.

Including this detection margin, the required system dynamic range can therefore easily exceed 100 dB. Such stringent dynamic range requirements place tight constraints on several radar building blocks, including phase-noise performance, chirp linearity, receiver linearity, compression behavior, and especially the analog-to-digital converter (ADC), for which the effective number of bits (ENOB) and linearity are critical design parameters.

Table 3.2: Typical radar cross section (RCS) values for common objects.

Object	**RCS (dBsm)**	**Notes**
Small bird, e.g., pigeon	−10 to −5	Strongly frequency-dependent
Child	−5 to 0	Varies with posture and movement
Human torso	−5 to 0	Depends on clothing and posture
Passenger car, broadside	10 to 20	Larger for trucks or vans
Motorcycle	5 to 10	Smaller frontal RCS
Truck	20 to 30	High reflectivity

3.5 Derivation of Radar Spectra in the Presence of a Frequency Deviation[1]

The high dynamic range requirements of FMCW radar systems require a thorough understanding of chirp frequency deviations and the manner in which different spectral components of these deviations influence system performance. Chirp impairments can generally be classified into two categories: random deviations and systematic deviations.

The most prominent random deviation is phase noise, which manifests as stochastic variations in the instantaneous frequency. These random fluctuations elevate the receiver noise floor and thereby limit the achievable dynamic range of the FMCW radar system. Unlike systematic deviations, the impact of random deviations can be mitigated through repeated coherent averaging.

[1]The rest of the chapter is based on the authors own work

Systematic frequency deviations, on the other hand, may manifest either as discrete spurious tones (spurs) or as a broadband-like noise floor. Spurs appear as discrete spectral components and can produce ghost targets, i.e., false detections that exist only within the radar system itself. Ideally, spur levels should remain below the radar dynamic range or be located outside the range of interest. Broadband systematic frequency deviations can also occur, producing a noise floor similar to quantization noise (QN) in analog-to-digital converters (ADCs), although their spectral distribution is not necessarily white. Such deviations may therefore become a limiting factor for the achievable radar dynamic range. In contrast to random deviations, the effects of systematic frequency deviations cannot be reduced through coherent averaging.

The prevailing benchmarking methodology in the literature relies on measuring the chirp frequency deviation in the time domain and reporting the corresponding root-mean-square (RMS) value. However, this approach suffers from several important shortcomings. First, presenting a time-domain plot of the frequency deviation together with its RMS value provides little insight into whether spurious tones will appear in the radar intermediate-frequency (IF) spectrum, whether the quantization-noise-like distortion is concentrated at low or high frequencies, or whether it exhibits a spectrally white characteristic. In other words, the RMS value neglects the spectral distribution of the chirp frequency deviation.

Second, in several published works [15, 16, 17, 18, 19, 20, 21, 22, 23], the integration bandwidth of the frequency error spectrum is not explicitly stated, leaving the reader uncertain regarding how much of the spectrum is included in the RMS calculation and how the selected bandwidth affects the reported result. Finally, even when the integration bandwidth is specified, the type and order of the filter applied to the time-domain frequency error are sometimes omitted [24], making reproduction and interpretation of the results difficult.

To address these limitations, this work presents an analytical framework for evaluating the impact of different spectral components of chirp frequency deviation on radar system performance. Furthermore, a benchmarking methodology is proposed that overcomes the shortcomings of the currently prevailing RMS-based approach.

3.5.1 Derivation of the Impact of a Modulation Signal on an Ideal Chirp

The transmitted (Tx) signal can be expressed as:

$$\mathrm{Tx}(t) = \sin\left(\omega t + at^2 + m(t)\right) \tag{3.11}$$

where ω is the angular frequency of the carrier, a is the chirp coefficient, and $m(t)$ is the added modulation term.

The received (Rx) signal is a time-delayed version:

$$\mathrm{Rx}(t) = \sin\left(\omega(t-\tau) + a(t-\tau)^2 + m(t-\tau)\right) \tag{3.12}$$

where τ is the time delay.

The intermediate frequency (IF) signal is obtained by mixing the transmitted and received signals:

$$V_{\mathrm{IF}}(t) = V_{\mathrm{Tx}}(t) \cdot V_{\mathrm{Rx}}(t) \tag{3.13}$$

After mathematical simplifications, we obtain:

$$V_{\mathrm{IF_low}}(t) = \frac{1}{2} \cdot \cos\left(2a\tau t + (m(t) - m(t-\tau))\right) \tag{3.14}$$

where high-frequency components from mixing are removed and constant phase terms are neglected as they do not affect subsequent analysis.

Assuming $m(t)$ is small, applying the narrowband FM approximation results in:

$$V_{\mathrm{IF_low}}(t) \approx \frac{1}{2} \left(\cos(2a\tau t) + (m(t) - m(t-\tau)) \cdot \sin(2a\tau t)\right) \tag{3.15}$$

To make the transition from the time domain to the frequency domain clearer, first consider the difference between the modulation of the transmitted signal and that of the delayed received signal:

$$\Delta m(t) = m(t) - m(t-\tau). \tag{3.16}$$

If $M(\omega)$ denotes the Fourier transform of $m(t)$, the time-shift property gives

$$\mathcal{F}\big[m(t-\tau)\big] = M(\omega)e^{-j\omega\tau}. \tag{3.17}$$

The Fourier transform of the modulation difference is therefore

$$\mathcal{F}\big[m(t) - m(t-\tau)\big] = M(\omega)\left(1 - e^{-j\omega\tau}\right). \tag{3.18}$$

Thus, the delay between the transmitted and received signals introduces the frequency-dependent factor

$$1 - e^{-j\omega\tau}. \tag{3.19}$$

The modulation difference in 3.15 is multiplied by $\sin(2a\tau t)$. Multiplication by a sinusoid in the time domain shifts the corresponding spectrum in the frequency domain. Consequently, the modulation spectrum is shifted to the positive and negative IF beat frequencies at $2a\tau$ and $-2a\tau$, respectively. This gives

$$\begin{aligned} F(\omega) = \frac{1}{2j}\Big[& M(\omega - 2a\tau)\left(1 - e^{-j(\omega-2a\tau)\tau}\right) \\ & - M(\omega + 2a\tau)\left(1 - e^{-j(\omega+2a\tau)\tau}\right)\Big] \end{aligned} \tag{3.20}$$

Equation 3.20 contains two shifted copies of the modulation spectrum, centred around the positive and negative IF beat frequencies. Considering one of these sidebands, let $\Delta\omega$ denote the frequency offset from the corresponding IF beat frequency. The magnitude of the delay-dependent factor is then

$$\left|1 - e^{-j\Delta\omega\tau}\right| = \left|2\sin\left(\frac{\Delta\omega\tau}{2}\right)\right|. \tag{3.21}$$

This directly gives the radar transfer function:

$$|H(\omega)| = \left|2\sin\left(\frac{\Delta\omega\tau}{2}\right)\right| \tag{3.22}$$

Equation (3.22) is referred to as the radar transfer function and is, unsurprisingly, identical to the transfer function describing phase-noise modulation in FMCW radar systems [25]. Several important observations can be made. First, the transfer function depends only on the frequency offset from the IF beat frequency and the target distance through the delay τ. The origin of this behaviour can be understood from the term $m(t)-m(t-\tau)$. For slowly varying modulation, $m(t)$ and $m(t-\tau)$ are similar and therefore largely cancel. This cancellation is particularly strong for short target distances, where τ is small. Consequently, low-frequency deviations are strongly attenuated. When the radar transfer function is plotted, as illustrated in Figure 3.2, this behaviour becomes clear.particularly for short target distances where τ is small.

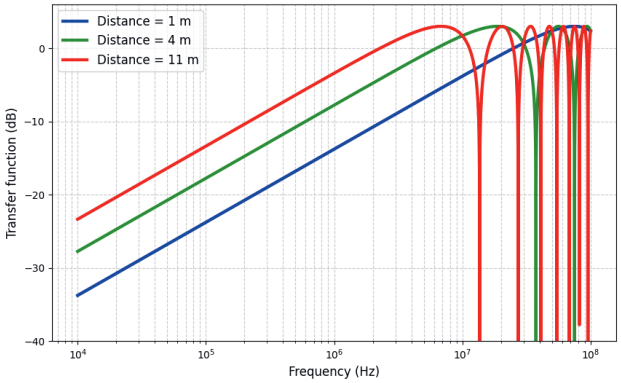


Figure 3.2: Illustration of the transfer function $20\log_{10}(|H(\omega)|)$ in (3.22) as a function of frequency for various target distance.

This observation has important design implications, since many analog circuit blocks, such as amplifiers, varactors, and phase detectors, predominantly exhibit low-order

nonlinearities. In contrast, mixed-signal building blocks, including digital-to-analog converters (DACs), sigma–delta modulators, and digital-to-time converters (DTCs), can introduce substantially higher-order frequency deviations.

The time-domain frequency error can be represented using a Fourier expansion, as shown in (3.23), where T_{chirp} denotes the chirp duration and $f_{\text{error}}(t)$ is assumed to be periodic over the interval $0 \leq t \leq T_{\text{chirp}}$.

$$f_{\text{error}}(t) = \sum_{n=1}^{\infty} \left(A_n \sin\left(\frac{2\pi n t}{T_{\text{chirp}}}\right) + B_n \cos\left(\frac{2\pi n t}{T_{\text{chirp}}}\right) \right) \tag{3.23}$$

The modulation term $m(t)$ is related to the frequency error through

$$m(t) = 2\pi \int_0^t f_{\text{error}}(t'), dt' + C \tag{3.24}$$

where C is a constant phase offset. From Eq (6), it follows directly how the different spectral components of $f_{\text{error}}(t)$ in (3.23) influence the radar system.

If a rectangular window is used during FFT-based radar processing, the first spectral null occurs at a frequency offset of $1/T_{\text{chirp}}$ from the carrier, corresponding to the FFT bin spacing. However, the rectangular window exhibits relatively large sidelobes, with the first sidelobe located approximately $-13\,\text{dB}$ below the carrier, followed by sidelobes at approximately $-18\,\text{dB}$, $-21\,\text{dB}$, and $-23\,\text{dB}$. Unless the low-order spectral components of the chirp frequency deviation are exceptionally large, these sidelobes will often dominate over the sidebands corresponding to spectral components with $n = 1, 2, 3$, or 4.

For this reason, rectangular windows are generally avoided in practical radar systems. Instead, windows such as the Blackman–Harris window are commonly employed. Although the Blackman–Harris window exhibits a broader main lobe than the rectangular window, thereby reducing range resolution, it provides significantly improved sidelobe suppression. The first null of the Blackman–Harris window occurs at a frequency offset of $4/T_{\text{chirp}}$. Consequently, if a Blackman–Harris window is applied and the chirp frequency deviation contains spectral components with order $n = 4$, ghost targets will typically not appear. Instead, the target response will merely broaden slightly, resulting in a modest reduction in range resolution.

For this reason, it is advisable to exclude frequency components below $4/T_{\text{chirp}}$ when calculating RMS frequency error. In addition, low-frequency noise further broadens the signal spectrum, thereby reducing the likelihood that the first few modulation sidebands appear outside the carrier main lobe. In many practical systems, the first significant ghost targets therefore arise from spectral components with orders $n = 5$ or $n = 6$. Furthermore, low-order frequency deviations are additionally attenuated by the radar transfer function in (3.22). As a result, the lowest-order modulation

terms often have negligible impact on radar performance unless the corresponding error amplitudes are exceptionally large.

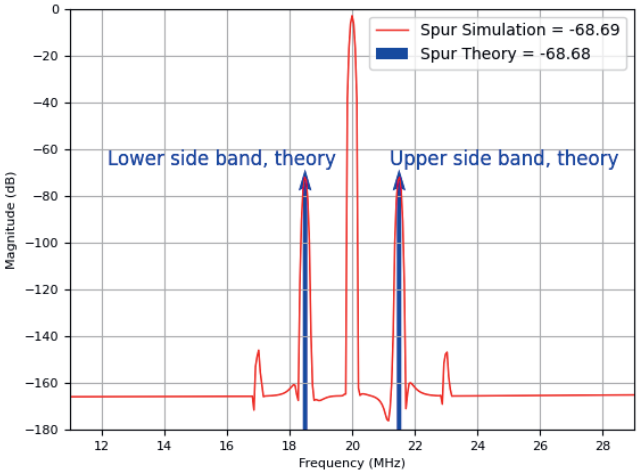


Figure 3.3: Comparison of MATLAB simulation with theoretical formula, (3.22).

3.5.2 MATLAB Verification of Analytical Model

The analytical model from Equation 3.20 is verified using a MATLAB simulation. A modulation term $m(t)$ with a modulation order of 30 is added to an ideal chirp. The amplitude of the modulation term is 0.001, and the chirp duration T_{chirp} is 20 μs. The chirp is swept from 76 GHz to 81 GHz, resulting in a 5 GHz chirp bandwidth. The target is located 12 meters from the radar. The simulation applies a Blackman-Harris window and is normalized such that the carrier has a 0 dB reference level.

The modulation term results in upper and lower sidebands that are 1.5 MHz apart from the carrier, as shown in Equation 3.20. By applying Equation 3.22, it is clear that the power of the sideband is calculated to be −68.68 dBc. The IF spectrum of the radar simulation is shown in Figure 3.3. The results demonstrate good agreement with the theoretical predictions from Equations 3.20 and 3.22, where the modulation term appears as a spur with the correct offset frequency and amplitude.

3.6 Limitation of Current Benchmarking Approach

This section presents three examples that demonstrate scenarios in which the commonly used benchmarking methodology for linear frequency chirps exhibits poor correlation with actual radar system performance. By jointly analyzing the time-domain

frequency error, the intermediate-frequency (IF) spectrum, and the spectrum of the frequency error itself, the limitations of the conventional RMS-based evaluation approach become evident.

3.6.1 Example I

Interpreting the spectral content of a chirp solely from time-domain plots can be challenging. Figure 3.4 illustrates this limitation. The upper plot shows the frequency error of a chirp over a 52 MHz bandwidth, with an RMS frequency error of 40 kHz, a value that would typically be considered excellent in literature comparisons [26]. However, the IF spectrum shown in Figure 3.4 reveals a significant spur located close to the carrier, corresponding to ghost targets at approximately −50 dBc relative to the main target, which is clearly unacceptable in most practical radar applications.

In Figure 3.4, the target is located 18 m from the radar, and the chirp duration is $T_{\text{chirp}} = 20\,\mu\text{s}$, resulting in a frequency-bin spacing of 5 kHz. The added modulation term has order $n = 40$ and amplitude 0.005, for a chirp sweeping from 76 GHz to 81 GHz. The frequency-error spectrum is plotted from 1 MHz to 100 MHz on a logarithmic frequency axis and clearly exhibits a dominant spur at approximately 2 MHz. The IF spectrum is normalized to 0 dB, thereby emphasizing the relative magnitude of the unwanted spectral component.

The approximately 10 dB-per-decade slope observed in the frequency-error spectrum is characteristic of white phase-noise behavior. If the modulation term $m(t)$ is spectrally white, the corresponding frequency error $f_{\text{error}}(t)$ is obtained through differentiation of $m(t)$, resulting in a spectrum with a 10 dB-per-decade slope. This frequency-domain representation provides substantially greater diagnostic insight than either the IF spectrum or the time-domain frequency-error waveform alone, making it a more effective tool for analyzing the impact of chirp nonidealities on radar system performance.

3.6.2 Example II

In several published works, the IF spectrum is either measured or simulated directly from time-domain frequency-error data [23, 27]. Example 2 demonstrates that, under certain conditions, the IF spectrum alone can be misleading if the measurement setup or signal conditions are unfavorable. Similarly, interpreting the spectral content solely from the time-domain frequency error may provide limited insight into the actual radar-system behavior.

Figure 3.5 illustrates this point. The upper plot shows the frequency error of a chirp over a 52 MHz bandwidth. The target is located 22 m from the radar, and the chirp duration is $T_{\text{chirp}} = 19.94\,\mu\text{s}$, corresponding to a frequency-bin spacing of approximately 5 kHz. The added modulation term has an amplitude of 0.02 and a modulation order of $n = 136$. The chirp sweeps from 76 GHz to 81 GHz.

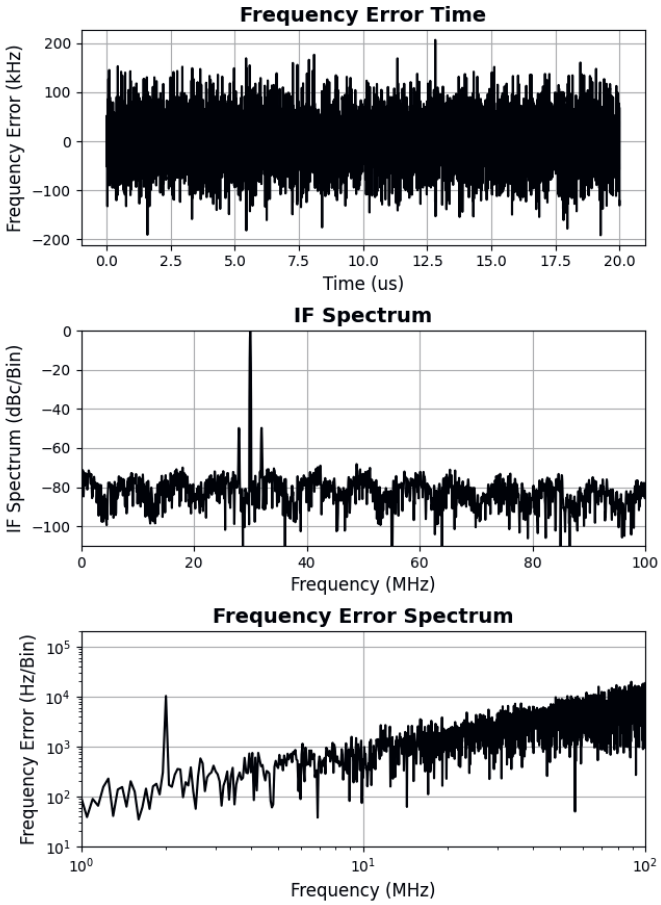


Figure 3.4: Frequency error in time domain, IF spectrum, and frequency deviation spectrum for Example I.

Based on these parameters, one would expect a prominent spur at an offset of approximately 6.82 MHz from the carrier, corresponding to a ghost target at approximately 36.7 m. However, inspection of the IF spectrum in Figure 3.5 reveals no such spur. This occurs because the spur is intentionally positioned at the first null of the radar transfer function, a result that can be readily verified using (3.22). In contrast, the

spur is clearly visible in the frequency-error spectrum shown in Figure 3.5.

This example demonstrates that the IF spectrum, range profile, and frequency-error spectrum must be analyzed jointly in order to accurately assess the performance of a generated chirp signal. Relying on only one of these representations may lead to incorrect conclusions regarding the impact of chirp nonidealities on radar-system performance.

3.6.3 Example III

Example 3, shown in Figure 3.6, demonstrates a case in which the frequency deviation is concentrated predominantly at low frequencies. In a conventional literature comparison, the chirp in Figure 3.6 would appear to exhibit poor performance because the RMS frequency error is relatively large due to significant low-frequency deviations. However, as discussed previously, low-order spectral components can often be excluded from the RMS calculation, while the remaining low-frequency components are additionally attenuated by the radar transfer function in (7).

The most demanding radar dynamic-range scenario typically occurs when a large target is located close to the radar while a much smaller target is positioned farther away. In such cases, the required dynamic range can easily exceed 100 dB [28], as predicted by the radar equation, where the received power scales inversely with the fourth power of the target distance.

In Figure 3.6, the IF spectrum is shown for a target located 2 m from the radar. Despite the relatively large RMS frequency error, the resulting radar-system performance remains excellent, as evidenced by the IF spectrum. Comparing Example 1 with Example 3, assuming the spurs in Example 1 are absent, shows that in a practical scenario involving a nearby large target and a distant weak target, the chirp in Example 3 actually outperforms the chirp in Example 1, despite having a significantly less favorable RMS benchmark value.

Once again, the frequency-error spectrum, together with the IF spectrum, provides substantially greater insight into actual radar-system performance than the RMS value alone. A design reported in the literature that resembles the behavior of Example 3, although to a somewhat lesser extent, is presented in [29]. That work appears to suffer from unfavorable benchmarking because visual inspection of the time-domain frequency error reveals that a substantial portion of the RMS value is concentrated at low frequencies, similarly to Example 3. Under a more realistic and application-oriented benchmarking methodology, the design in [29] would likely appear significantly more competitive.

This observation warrants further discussion because such a frequency-error spectral distribution is likely common in chirps generated using phase-locked loops (PLLs) [16]. In PLL-based chirp generators, high-frequency deviations are naturally attenuated by the PLL loop filter. Consequently, the limited loop bandwidth often results in predominantly low-order frequency deviations.

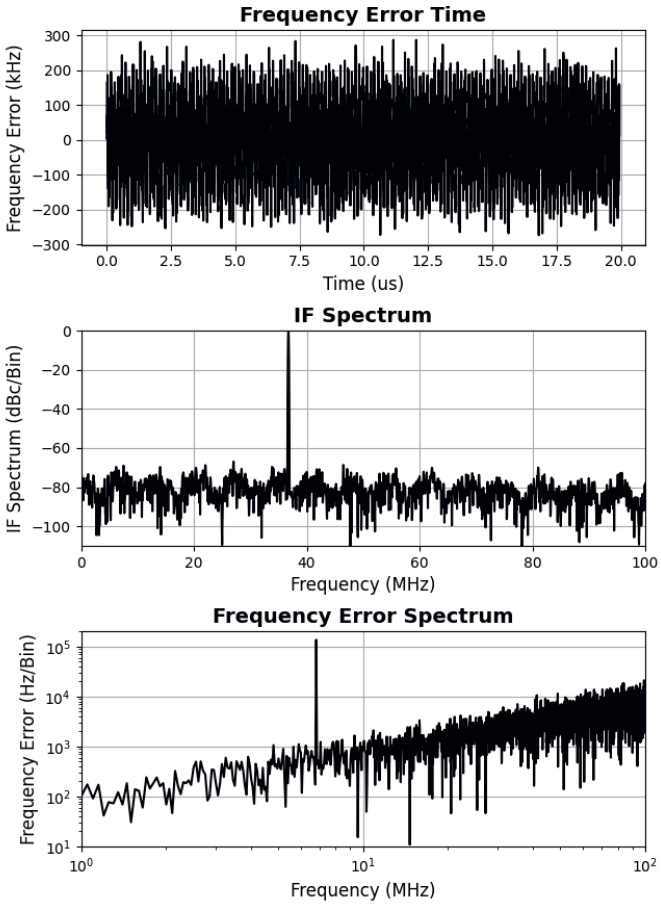


Figure 3.5: Frequency error in time domain, IF spectrum, and frequency deviation spectrum for Example II.

One example in which considerable design effort is devoted to suppressing low-order spurs is presented in [16]. However, the preceding analysis raises the question of whether such effort is always justified from a radar-system perspective. In contrast, the approaches presented in [24, 27, 30] appear to suppress harmonic components at frequencies sufficiently high that the resulting spectral components may lie outside the

IF bandwidth entirely. Such approaches can only be justified if the sole optimization objective is minimizing the total RMS frequency error, despite the fact that this metric may correlate poorly with realistic radar-system performance.

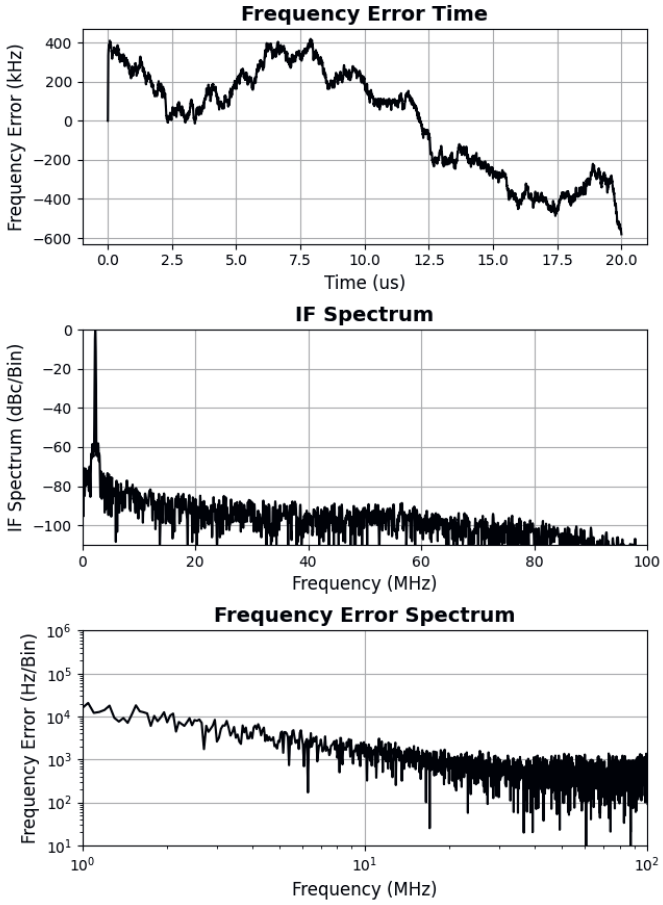


Figure 3.6: Frequency error in time domain, IF spectrum, and frequency deviation spectrum for Example III.

3.7 Proposed Benchmarking Approach

Examples I–III illustrate why simply reporting the time-domain frequency error can be misleading. Much more insight is gained by plotting the spectrum of the frequency error. Since the frequency error often varies by three orders of magnitude across the IF bandwidth, it is recommended to plot the error using a log scale.

Another source of inconsistency is that the frequency error is passed through a filter, and the order and shape of this filter can have a measurable impact on the reported RMS value. This leads to inconsistencies and inaccuracies between different publications.

The following benchmarking method is proposed:

1. Plot the spectrum of the frequency error.
2. Determine the lowest frequency of interest—most likely the chirp frequency or a higher frequency depending on the desired distance range.
3. Determine the maximum distance/range of interest and calculate the corresponding IF of interest.
4. Calculate the RMS value of the spectrum from the lowest to the highest frequency of interest. Essentially, the bins outside the frequency range of interest are filtered with a brick-wall filter.

If the frequency error is defined at the zero crossings, this can be done using the non-uniform Fourier transform or by interpolation onto a uniform time grid, followed by a Fourier transform.

3.8 Local Oscillator Distribution Architecture

Continuous-time radar systems require full-duplex operation, which presents a significant challenge due to typically low antenna isolation at D-band frequencies. For example, the antenna array described in [31] achieves only 20 dB of isolation between the transmit (Tx) and receive (Rx) antennas.

The problem becomes more severe in MIMO radar systems. For instance, in a 4-Tx/4-Rx MIMO configuration, each receiver may experience spillover from four relatively strong transmit signals. If a 0 dBsm RCS target is located 1 meter from the radar, the radar equation (3.22) shows that the spillover or crosstalk can be up to 60 dB stronger than the actual power from the target.

This has critical implications for local oscillator (LO) generation and chirp synthesis. If the phase noise and chirp signals are uncorrelated between the transmit and receive paths, the spillover can, severely limiting the radar system's dynamic range.

However, if the radar system is highly correlated, the radar transfer function (3.22)

effectively down-converts the phase error to near-DC, where it can be filtered out using a simple RC high-pass filter. As the time difference between the spillover signal and the signal reaching the receiver mixer is very small—for example, a delay of only 10 picoseconds—this corresponds to an approximate cutoff frequency of 100 GHz in the radar transfer function. This means the LO signal and chirp waveform must be generated centrally and then distributed across the chip, such that the frequency deviations in the chirp and the phase noise is highly correlated between the different receivers.

The remaining design question is: At what frequency should the LO and chirp signals be distributed? Figure 3.7 illustrates three different architectural options.

In Figure 3.7 (a), the oscillator and chirp are generated directly at the RF frequency. While this approach simplifies the architecture, it results in significantly higher power consumption due to the need to route high-frequency signals across the chip. This method may be feasible at W-band, but at D-band, the low quality factor (Q) of the LC tank severely limits performance.

In Figure 3.7 (b), the LO and chirp signals are generated and distributed at a lower frequency, then upconverted using a frequency multiplier placed near the power amplifier and mixer. This approach improves phase noise performance, as lower-frequency oscillators typically offer better spectral purity. Additionally, distributing signals at lower frequencies reduces overall power consumption.

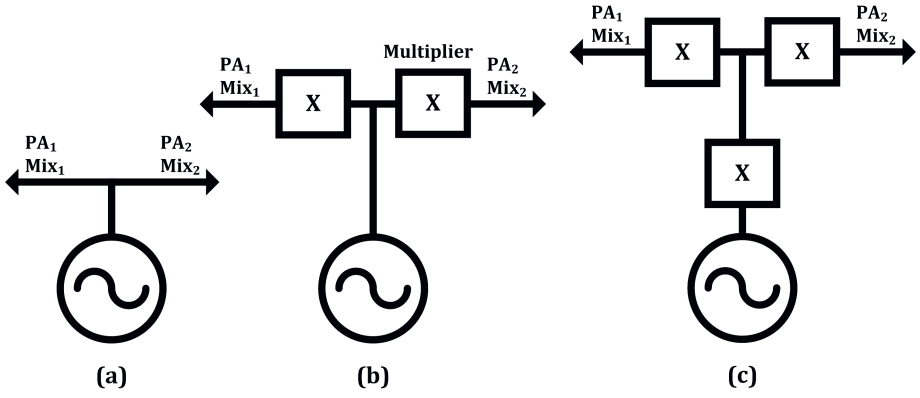


Figure 3.7: LO generation and distribution architectures for radar systems: (a) direct RF generation, (b) low-frequency LO generation and distribution with upconversion performed close to the mixer, (c) multi-step upconversion architecture.

Finally, Figure 3.7 (c) shows an architecture where the LO is generated at a low frequency and then immediately upconverted in a way that ensures the phase noise of the first frequency multiplier is correlated between the Tx and Rx paths. This

architecture has the advantage of cancelling or correlating more of the noise originating from the multiplier stage. However, this comes at the cost of increased power consumption due to the added complexity in the multiplier circuitry.

Finally, it is important to consider the implications of distributing the chirp using a high-gain, low-frequency amplifier—for example, if the chirp is generated at 8 GHz and then distributed and upconverted to W-band or D-band. An inverter operating at 8 GHz can produce a relatively strong third harmonic at 24 GHz, especially in modern CMOS technologies that lack inductive matching.

If this harmonic is not properly filtered, it can be downconverted in the receiver and appear as a ghost target at three times the actual range of the real target, provided it falls within the intermediate frequency (IF) bandwidth. This concern highlights the potential benefit of generating the chirp at a somewhat higher frequency than 8 GHz. At higher frequencies, the third harmonic shifts further out of band, making it easier to filter and reducing the risk of ghost target artifacts.

Chapter 4

Frequency Multiplication

In this chapter, a brief introduction to state-of-the-art frequency multipliers is presented. Injection-locked frequency multipliers and harmonic multipliers are discussed. A frequency multiplier topology that enables high voltage conversion gain and low power consumption is proposed.

4.1 Introduction

A straightforward approach is to directly generate the mm-wave carrier using a mm-wave voltage-controlled oscillator (VCO) and a phase-locked loop (PLL). However, designing a low phase noise VCO with a reasonable tuning range at these frequencies presents significant challenges, primarily due to the limited quality factor of varactors and switches at mm-wave frequencies. These challenges are further exacerbated by the stringent requirements of millimeter-wave systems, such as those discussed in Chapters 2 for 5G FR2 and high-performance radar applications discussed in Chapters 3. Consequently, it may be necessary to implement the oscillator at a lower frequency.

Furthermore, distributing the signal over long distances at RF frequencies can be prohibitively power-intensive. As discussed in Chapters 2 and 3, an alternative approach involves implementing a phase-locked loop (PLL) at a lower frequency and subsequently employing frequency multipliers, positioned near the mixers, to achieve the desired carrier frequency.

As highlighted in Chapters 2 and 3, the frequency multiplier is a highly versatile block. This motivates the study and implementation of efficient frequency multipliers.

4.2 State of the art

Broadly, one can divide frequency multiplication into three approaches: cascaded PLLs, injection-locked multipliers, and harmonic frequency multipliers. Cascaded PLLs will be discussed in Chapter Five.

4.2.1 Injection looked frequency multipliers

When an oscillating signal is injected into an oscillator, and the frequency of the injected signal is sufficiently close to that of the oscillator, the oscillator can become *injection-locked*, meaning it synchronizes to the exact frequency of the injected signal. This locking occurs only when the frequency offset is within a certain range, known as the locking range. The locking range f_L for an LC-tank-based oscillator is given by Equation (4.1) [32].

$$f_L = \frac{f_0}{2Q_{\text{tank}}} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\sqrt{1 - \left(\frac{I_{\text{inj}}}{I_{\text{osc}}}\right)^2}} \tag{4.1}$$

Injection locking can also occur when the injected signal is near a subharmonic of the oscillator's frequency, in which case it is referred to as subharmonic injection locking.

The phase noise dynamics of a locked system are given by Equations (4.2), (4.3), and (4.4) [33]. Where $H_{rl}(j\omega)$ and $H_{up}(j\omega)$ are the transfer functions for the VCO and the reference signal, respectively. Here, β is the realignment factor, a measure

of how much the injected signal can phase-shift the oscillator. ω is the offset angular frequency, N is the multiplication factor (the integer difference between the injected signal frequency and the oscillator frequency), and T_r is the reference clock period.

$$\theta_{\text{inst_vco}}(j\omega) = \theta_{\text{vco}}(j\omega)H_{rl}(j\omega) + \theta_{\text{ref}}(j\omega)H_{up}(j\omega) \tag{4.2}$$

$$H_{rl}(j\omega) = 1 - \frac{\beta}{1 + (\beta - 1)e^{-j\omega T_r}} e^{-j\omega T_r/2} \frac{\sin(\omega T_r/2)}{\omega T_r/2} \tag{4.3}$$

$$H_{up}(j\omega) = \frac{N\beta}{1 + (\beta - 1)e^{-j\omega T_r}} e^{-j\omega T_r/2} \frac{\sin(\omega T_r/2)}{\omega T_r/2} \tag{4.4}$$

Once synchronization is achieved, the low-frequency phase noise of the oscillator is significantly suppressed (4.3). Meanwhile, the phase noise from the reference is upconverted to the oscillator (4.4). The overall dynamics resemble those of a Type-I PLL, as the phase noise of the oscillator is suppressed with approximately one pole [34].

Injection locking exhibits the desirable property of high conversion gain when the injected frequency is close to the free-running oscillator frequency. Under this condition, a high voltage or power gain can theoretically be achieved even when the injected signal amplitude is very small. However, several practical limitations must be considered. If the frequency difference between the oscillator and the injected signal is too large, locking may fail to occur, making this method less robust under varying PVT conditions. Moreover, achieving reliable lock often requires additional complex acquisition circuits, which increase design complexity and simulation time [35]. Additionally, the injection-locked oscillator can be susceptible to pulling effects from the power amplifier, which may degrade spectral purity. This pulling can have a disastrous effect on system performance [32]. Additionally, injection-locked oscillators have a larger phase noise budget compared to multipliers, and this phase noise budget involves a trade-off with conversion gain.

4.2.2 State of the art harmonic multipliers

A conventional push-push frequency doubler is illustrated in Figure 4.1,(a). This topology offers advantages such as low circuit complexity and efficient power utilization. However, the conventional doubler topology, that is shown in Figure 4.1 (a), suffers from a number of shortcomings.

The output swing is constrained due to the single-ended nature of the first stage. In addition, the use of the single to differential transformer introduces challenges. Specifically, it requires careful consideration of the return path from supply to ground, as illustrated in Figure 4.2(a). When this return path spans a significant portion of

the layout, accurately predicting its impact on performance becomes difficult and demands computationally intensive electromagnetic (EM) simulations.

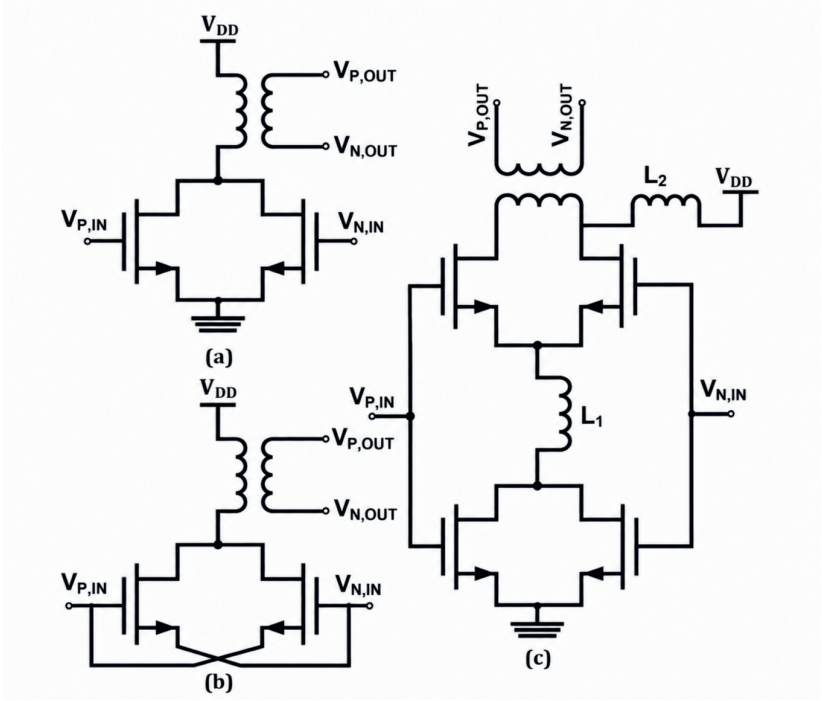


Figure 4.1: Schematics of: (a) Conventional push-push doubler (b) Doubler using common gate topology (c) Efficient frequency tripler.

Furthermore, the transformer must be precisely balanced. As shown in Figure 4.2(b), any imbalance results in a common-mode signal at the output, which negatively affects the frequency multiplier's conversion gain. Designing a well-balanced transformer at mm-wave frequencies—such as in the D-band is particularly challenging, especially when additional requirements such as inductive matching must also be satisfied. Moreover, single-ended transformers tend to have a lower quality factor than their differential counterparts, further limiting performance.

Another proposed frequency doubler is shown in Figure 4.1(b) [36]. This design suffers from similar issues as the topology in Figure 4.1(a). Additionally, it exhibits a low input impedance due to the use of a common-gate transistor configuration. While this can be beneficial for achieving power gain, it is a major disadvantage when it comes to achieving a high voltage gain.

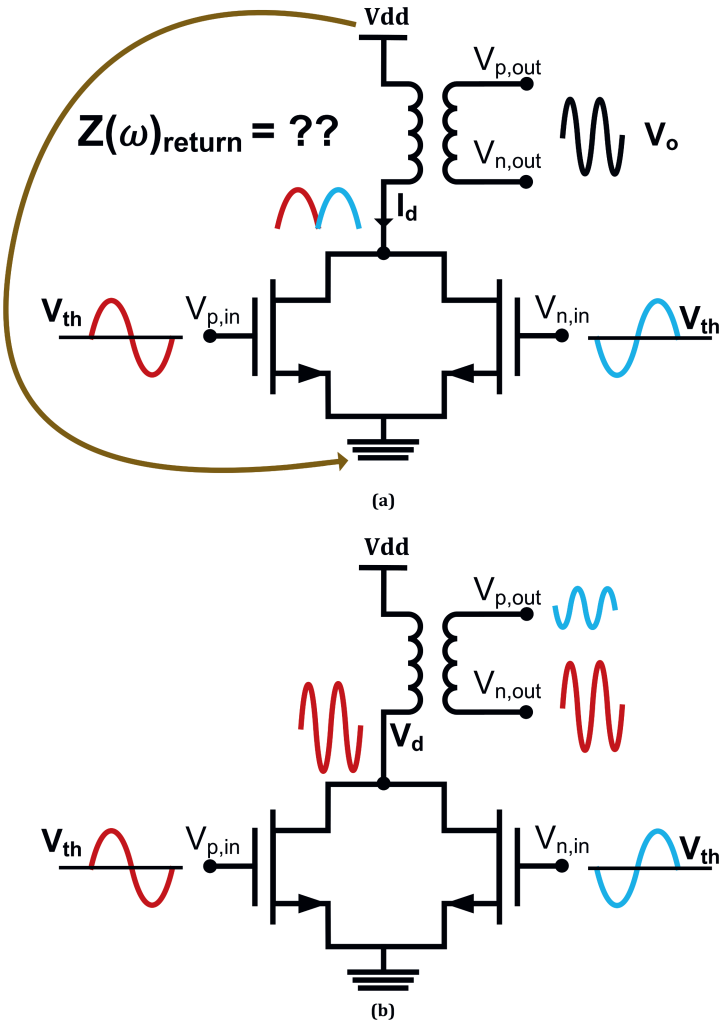


Figure 4.2: Issues with Conventional push-push doubler: (a) Return path (b) Transformer imbalance.

The frequency tripler shown in Figure 4.1(c) was first proposed in [37]. The implementation in [37] is slightly different from the one depicted in Figure 4.1(c). In this topology, the lower transistor pair functions as a push-push doubler, generating a strong second harmonic voltage at the source node of the mixing pair. This second harmonic is then mixed with the fundamental input signal to produce the third harmonic at the output.

As demonstrated in [38], when inductors L_1 and L_2 are tuned to resonate at the second harmonic of the input frequency, the second harmonic voltage at the mixer source is maximized. This resonance condition enhances the mixing efficiency and significantly boosts the conversion gain.

This architecture addresses several limitations of conventional push-push doubler in Figure 4.2(a). It offers a fully differential output by employing a differential transformer, thereby mitigating issues related to transformer imbalance and enabling higher output voltage swing.

However, this approach comes with trade-offs. It requires a transformer and two inductors, which increase the circuit's area consumption. While the design is power-efficient, with a moderate current consumption of only 7.8 mA at 140 GHz output frequency, the voltage conversion gain remains relatively low, reaching only –5 dB [38].

4.2.3 Benchmarking

Unfortunately, benchmarking approaches for harmonic multipliers and injection-locked multipliers vary significantly, making direct comparisons difficult. Harmonic multipliers are typically evaluated based on metrics such as drain efficiency, output power, power gain, multiplication ratio, and overall power consumption. In contrast, injection-locked oscillators are generally benchmarked using power consumption, phase noise, and multiplication ratio.

However, before considering which benchmarking approach is most appropriate, it's essential to consider the role the frequency multiplier plays in the system. For instance, when a multiplier directly drives a power amplifier (PA), it is appropriate to assess performance in terms of power amplification, drain efficiency, and power consumption. However, when the objective shifts to driving a mixer, in a receive or transmit path, it becomes crucial to provide sufficient voltage swing.

Voltage gain cannot be directly measured; only power gain can be measured directly. This necessitates matching the harmonic multiplier to a 50-ohm load, which significantly increases power consumption. As a result, harmonic multipliers that are benchmarked under such conditions often exhibit higher power consumption, potentially leading to misleading comparisons with injection-locked multipliers.

If it is assumed that the frequency multiplier is intended to drive a mixer or another high impedance load. The most relevant performance metrics are voltage conversion gain, power consumption, and phase noise.

4.3 Proposed frequency doubler

The proposed doubler[1] in Figure 4.3, addresses many of these issues with the conventional push push doubler. First, the transformer is differential to differential,

[1]This doubler topology was proposed independently in [39] and [40].

mitigating problems associated with transformer imbalance and return path modelling issues. Second, the fully differential configuration allows for a higher saturation voltage. Third, efficiency is boosted by the current reuse feature (the flow of DC and AC currents is shown in Figure 4.3. Finally, the doubler has a high input impedance, yielding a higher voltage gain.

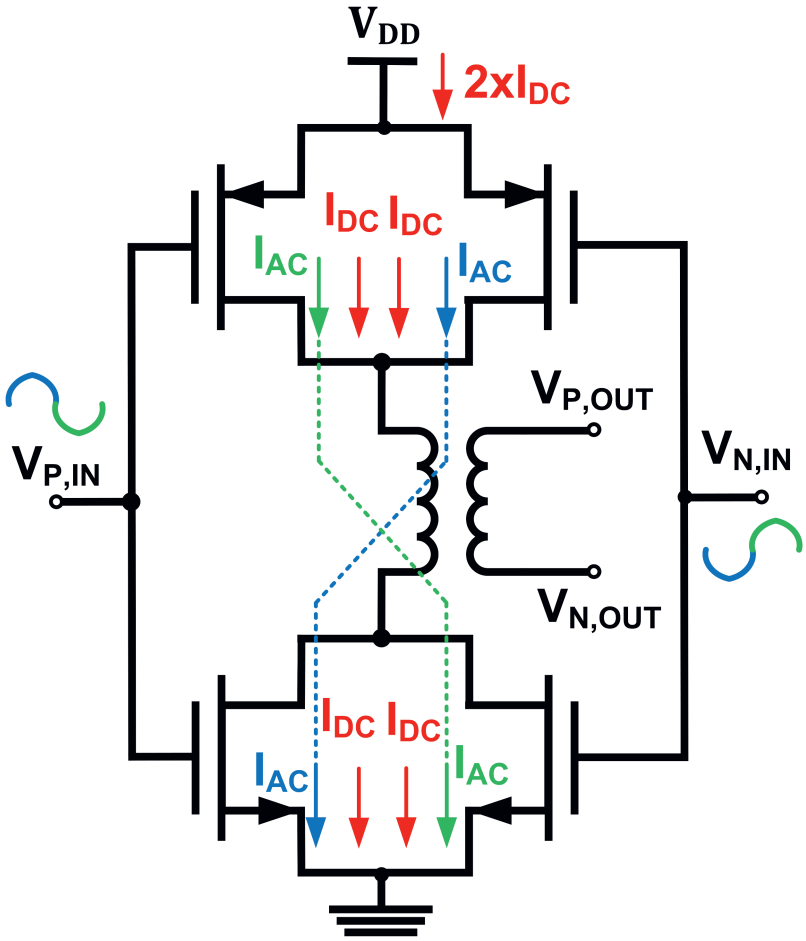


Figure 4.3: Proposed frequency doubler

4.3.1 Implemented doubler

In Figure 4.4, the schematic of the complete frequency upconverter is depicted. The first stage upconverts from 36 GHz to 72 GHz, while the second stage upconverts

from 72 GHz to 144 GHz. The output buffer is used to drive the pad capacitance providing sufficient swing for measurement purposes. The transistors employed in the frequency doublers (M1-M8) have the same aspect ratios 9um/30nm, while the aspect ratio of the transistors in the output buffer (M9-M10) is 8um/28nm. The circuit operates with a 900mV supply. The doublers consumes only 3.2 mW when operated in saturation. The bias voltage for the doubler is set to 350 mV matching the stronger nmos transistors with the weaker pmos transistors. Simulation shows that the doubler is relatively insensitive to changes in the bias voltage, when driven with sufficiently large input signal.

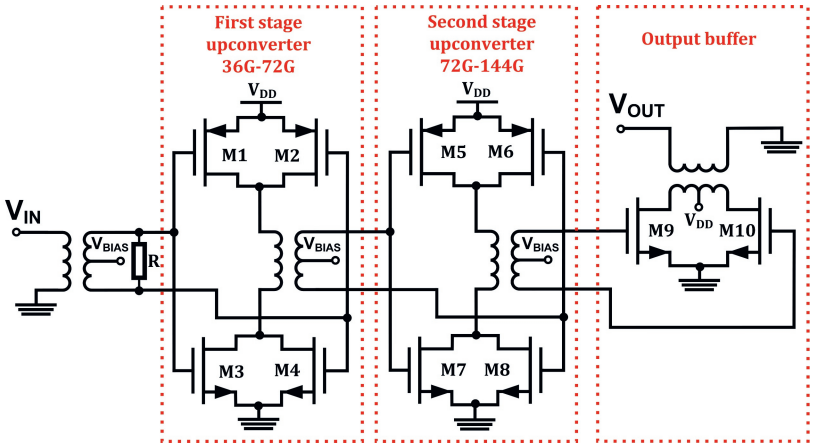


Figure 4.4: Schematic of proposed fully differential frequency upconverter by 4 followed by output buffer.

The frequency doublers are designed for a high voltage conversion gain and not for high power gain or high power efficiency. The selected transistor sizes are the result of the trade-off between achieving sufficiently large transistor transconductance and node impedance yielding maximum voltage gain (transconductance improves by increasing transistor size while node impedance decreases). It is surprising that such a trade-off is achieved using relatively small transistors. In order to alleviate the impedance matching at the input, a shunt 50-ohm resistor is used. This results in a deplorable power gain for the overall circuit, as most of the power goes into the resistor. The main goal here is to characterize the differential D-band doubler. The following approach is taken. The first step is to build correspondence between measured and simulated results for the full upconverter depicted in Figure 4.4. The second step is to characterize only the D-band doubler, by estimating its gain, bandwidth and phase noise from simulations. This somewhat unconventional approach is taken as the voltage gain of the doubler can't be directly measured.

4.3.2 Measurement

The multiplier by 4 is implemented in CMOS 28nm. Figure 4.5 shows the die photo together with the measurement setup.

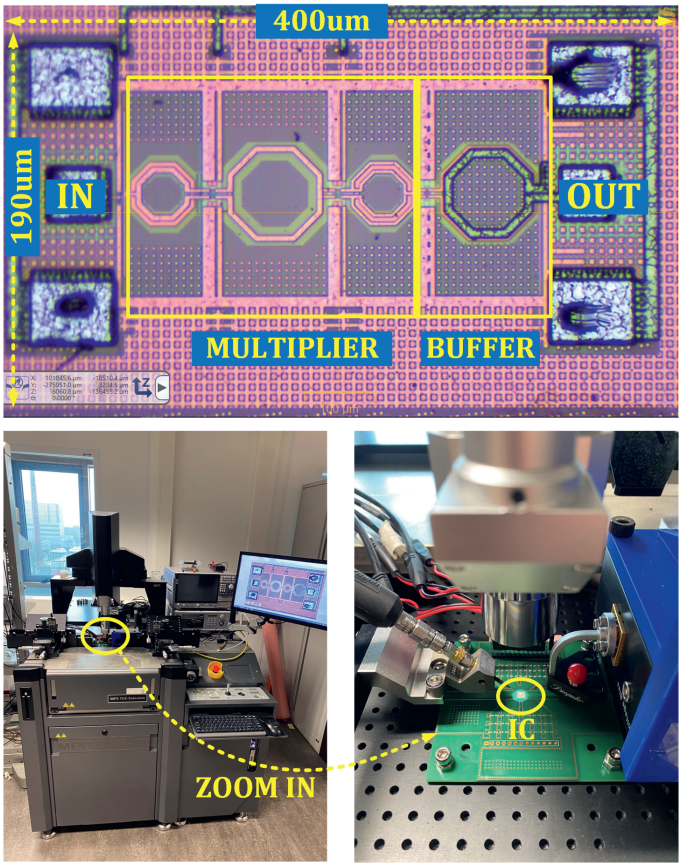


Figure 4.5: Chip photo and measurement setup.

The manufactured chips are measured through on-chip probing. The input signal source is taken from Anritsu MG36241A RF signal generator and the RF output is measured with a 4X downconverter extender, VDI Compact Down Converter (CCD) Model WR6.5CCD-M4. The signal is then fed into a Rohde and Schwarz FSW67 spectrum analyzer. The input cable and probe are calibrated with a Keysight PNA-X network analyzer. The calibration of the 4X down converting extender was done in two steps. Initially, the power meter VDI Erickson PM4 was connected directly to the circuit. In the second step the power meter was replaced with the 4X down converting extender and spectrum analyzer. By comparing the measured power levels,

the loss in the extender could be obtained. Initially, it was planned to carry out all the measurements using the power meter. Unfortunately, the power meter proved unreliable with low input power. Therefore, the power measurements are done using spectrum analyzer. S_{11} is measured with the network analyzer and S_{22} is measured with the 4X downconverter extender and the network analyzer.

Figure 4.6, shows the output power at 144 GHz plotted versus the input power at 36 GHz.

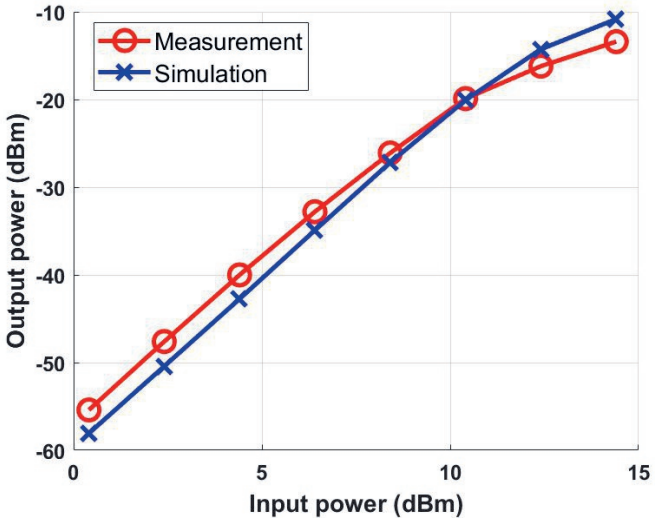


Figure 4.6: Measured and simulated power transfer characteristic of the frequency upconverter

Figure 4.7, shows the output power over frequency, where 13 dBm is the power of the 36 GHz signal injected into the circuit. The 3 dB bandwidth is 10 GHz.

Figure 4.8 and Figure 4.9 shows S_{11} and S_{22} over frequency, respectively. The frequency doublers consume 3.2 mW and the output buffer consume 4.4 mW when driven in saturation.

4.3.3 Simulations

Various simulations have been performed in order to evaluate performance of the proposed frequency upconverter. They are carried out using post-layout view of the active part (MOS transistors) together with the models of the transformers, which are obtained by EM simulations. Figure 4.10 shows the simulated transfer characteristic (output voltage versus input voltage) of the second stage of the frequency doubler, which converts, from 72GHz to 144GHz. Figure 4.11, shows the simulated large signal

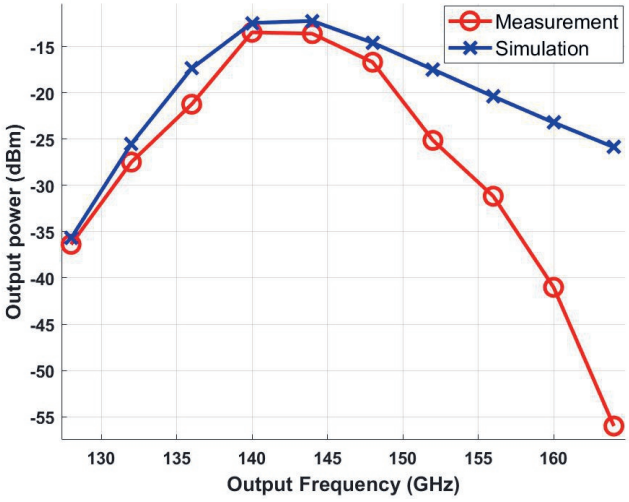


Figure 4.7: Measured and simulated output power of the frequency upconverter, versus frequency, when input signal with a power of 13 dBm is applied.

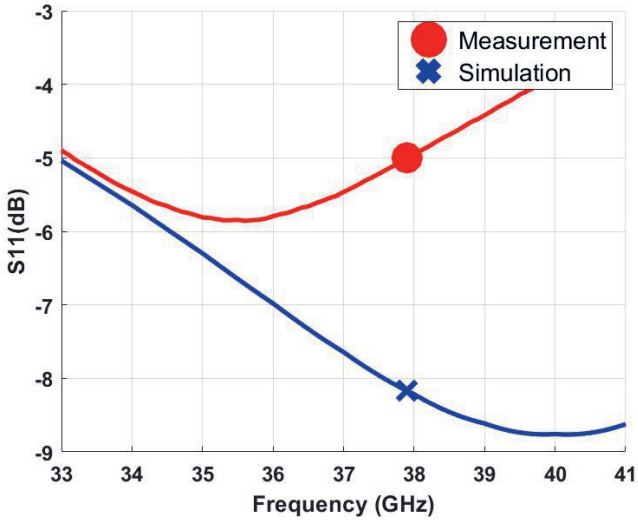


Figure 4.8: Measured and simulated S_{11} of the frequency upconverter.

voltage conversion gain of the same stage when driven with a 300-mV input signal. The 3 dB bandwidth is 11 GHz. Figure 4.12, shows the simulated phase noise of the

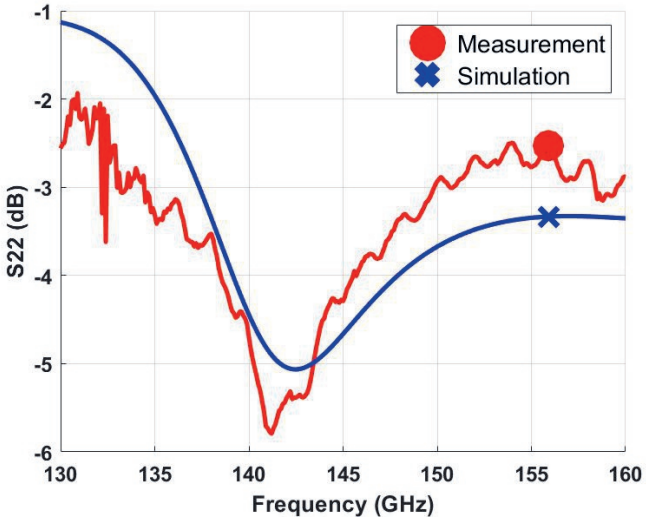


Figure 4.9: Measured and simulated S_{22} of the frequency upconverter.

second stage of the frequency upconverter when driven by 300mV input signal and at frequency of 144GHz. The phase noise is below state of the art PLL.

4.3.4 Transistor Modeling and Layout

Accurate active and passive modelling is incredibly important when designing at D-band. Typically, the RF-transistors in CMOS technologies are not characterized up to D-band frequencies. Consequently, models might not accurately capture the transistors high frequency behaviour. One approach is to tapeout stand-alone transistors, characterize them, compile into a library, and subsequently utilize them. An example of such approach can be found in [41]. While rigorous, this method is very labour intensive. Another approach is suggested in [42], the idea is to use the logic transistors (not RF-transistor) and extract all the parasitics including the lower metal layers with electromatic magnetic simulation tools (EM) such as (Electro-Magnetic eXtractor) EMX. In this design the logic transistors are used and the parasitics are extracted with rule-based parasitic extracting tools such as PEX. Extracting with PEX is less accurate than with EM tools, as PEX doesn't capture the frequency behaviour or the inductive contributions. However, it is simpler and deemed sufficient in this case.

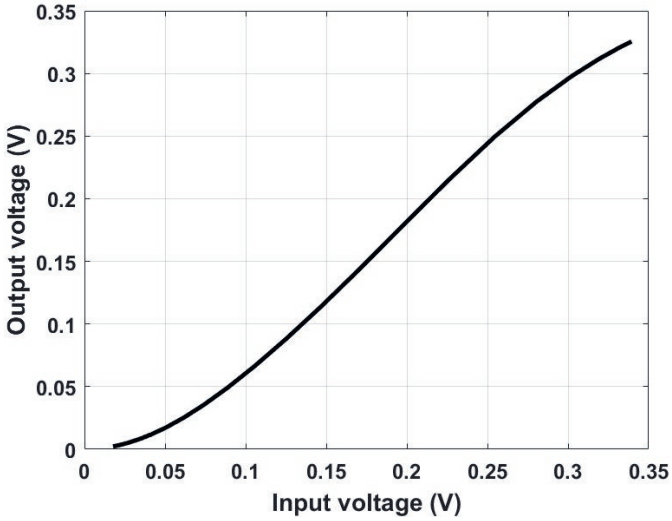


Figure 4.10: Simulated voltage transfer characteristic of the second stage of the frequency upconverter.

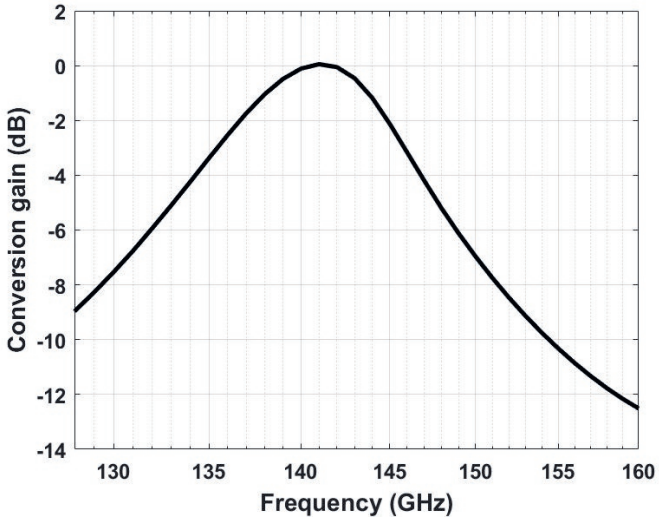


Figure 4.11: Simulated large signal voltage conversion gain of the second stage of the frequency upconverter when driven by 300mV input signal.

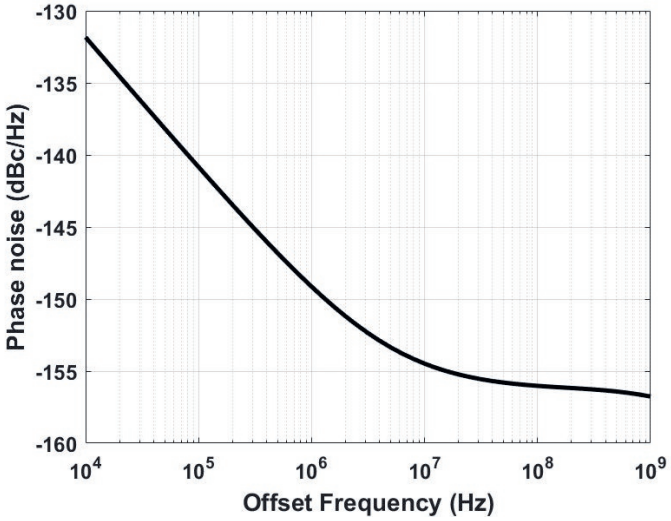


Figure 4.12: Simulated phase noise.

4.4 Discussion and Conclusion

This section discusses the results of the proposed doubler and compares its performance with other approaches reported in the literature. Based on this comparison, key observations and conclusions are drawn. In particular, three state-of-the-art approaches are discussed with reference to the comparison Table 4.1.

- **A 170-GHz 23.7% Tuning-Range CMOS Injection-Locked LO Generator With Third-Harmonic Enhancement [43]**
  This work presents a CMOS injection-locked local oscillator employing an enhanced third-harmonic technique. In this approach, the voltage-controlled oscillator (VCO) oscillates at f_o, while the third harmonic is significantly enhanced by tuning the resonant tank to exhibit an impedance peak at three times the fundamental frequency. This strategy enables injection locking to be performed at the fundamental frequency, where generating a sufficiently large injection signal is relatively straightforward. The proposed circuit achieves an impressive tuning range while maintaining moderate power consumption, as compared with other designs summarized in Table 4.1. However, the drain efficiency is lower than that of doubler and tripler architectures operating at similar frequencies.

- **An Ultra-Low Jitter, Low-Power, 102-GHz PLL Using a Power-Gating Injection-Locked Frequency Multiplier-Based Phase Detector [44]**
  This work presents a power-gated injection-locked PLL. The concept, first proposed in [45], relies on periodically powering down and up the VCO using a

reference clock signal. The paper proposes the use of two VCOs: one VCO is power-gated and injection-locked, and is therefore temporarily turned off during operation, while a second VCO operates continuously and is locked to the power-gated VCO.

The advantage of this approach is that a reference signal can be efficiently upconverted to the RF domain without requiring a large network of low-frequency PLLs and cascaded frequency multipliers.

- **A D-band low-power and high-efficiency frequency multiply-by-9 fmcw radar transmitter in 28-nm cmos [38]**
  A 3× frequency multiplier is implemented by placing a mixer stage on top of a push–push doubler. It is observed that the performance can be significantly improved by introducing a phase-alignment inductor at the source of the mixer. The resulting design achieves excellent drain efficiency; however, the voltage conversion gain is somewhat lower.

Looking at Table 4.1, the injection-locked frequency multiplier approach appears to exhibit lower drain efficiency and simultaneously higher power consumption than comparable harmonic frequency multipliers. Additionally, injection locking suffers from the issues discussed above, such as the need for calibration circuits to ensure robust locking and its susceptibility to pulling by the power amplifier. Potentially even more problematic, injection-locked multipliers exhibit a substantially higher phase-noise contribution than harmonic doublers, particularly when the input signal is small or when the multiplication ratio is high. This suggests that doublers or triplers are the more suitable choice for many communication and radar systems. However, if chip area is a significant constraint, as can be the case in antenna-in-package (AiP) implementations where the die must fit behind the antenna array, the PG injection-locking approach might become attractive, as it circumvents the need for large low-frequency VCOs.

The comparison between the doubler and tripler is more complex. For example, the harmonic tripler also demonstrates good drain efficiency and gain. The differences in gain and drain efficiency are most likely due to input and output loading rather than fundamental architectural limitations. The tripler requires two inductors and one transformer, while the doubler only requires a single transformer. However, the tripler performs an upconversion by a factor of three rather than two, which should be taken into account when comparing their performance and complexity.

The proposed doubler has several advantages. The doubler employs a current-reuse structure, allowing for the utilization of a differential-to-differential transformer. This configuration helps achieve state-of-the-art voltage conversion gain. The achieved 0 dB voltage conversion gain is, to the authors' knowledge, the highest reported around D-band frequencies in CMOS technologies. Additionally, the proposed doubler is very simple to implement. The low power consumption and low phase noise make the proposed architecture a promising choice for carrier generation and distribution in

high-performance radar and communication systems.

Table 4.1: Comparison of state of the art.

Parameter	**This Work**	**[43]**	**[44]**	**[38]**	**[40]**
Architecture	Harmonic doubler	Injection locked VCO	PG-Injection locked PLL	Harmonic tripler	Harmonic doubler
Process	28 nm	65 nm	65 nm	28 nm	40 nm
Center Frequency (GHz)	144	175	101	145	138
Multiplication factor	2	3	199-205	3	2
Drain efficiency	0.83 %	0.41 %	NA	4.2 %	1.33 %
DC Power (mW)	1.6	8.3	22	7.8	41.4
Voltage gain (dB)	0	NA	NA	-5.2	NA
3dB Bandwidth (GHz)	10	41	3	NA	14
Area (mm^2)	0.014	0.08	0.16	NA	0.04

Chapter 5

Fractional-N Phase Looked Loop

In this chapter, a brief introduction to phase-locked loops (PLLs) is presented, along with a short overview of the state of the art. Furthermore, explicit closed-form formulas for the spurs resulting from non-linearities in fractional-N PLLs are derived. A theoretical study of the impact on spurs using several sigma–delta modulators operated in parallel is conducted, and several insights are presented. A PLL design is also proposed, highlighting a highly linear pseudo-differential digital-to-time converter.

5.1 Introduction

This chapter addresses the implementation details of the fractional-N PLL and effectively continues where Chapter 2 concluded. While the design considerations required to achieve very low phase noise at the system level were discussed previously, this chapter focuses on the practical implementation aspects of the fractional-N architecture in greater detail.

In particular, quantization noise and fractional spurs are analyzed comprehensively. Closed-form expressions for the magnitude of fractional spurs are derived using the proposed PNN theory. Furthermore, the concept of employing multiple phase-shifted sigma–delta modulators operating in parallel is investigated in detail as a method for suppressing fractional spurs and reducing the impact of nonlinearities.

In addition, a pseudo-differential DTC architecture is proposed to address linearity limitations without compromising the noise–power tradeoff. The proposed DTC is implemented in a 28 nm bulk CMOS technology, and the most important circuit building blocks are discussed in detail. A novel phase-extraction circuit is also proposed, and the measurement results of the fabricated prototype are presented and the measurement results are discussed in detail..

5.2 Fractional-N PLL

A basic fractional-N PLL architecture is shown in Figure 5.1. The phase detector compares the phase difference between the reference signal and the divided VCO output. This phase error is then converted into a control signal that adjusts the oscillator frequency, thereby forcing the PLL into lock. In the locked state, the output frequency is equal to the reference frequency multiplied by the division ratio.

In an integer-N PLL, the division ratio is constant, and therefore the output frequency can only be an integer multiple of the reference frequency. However, many applications require finer frequency resolution. To achieve this, the divider ratio can be modulated such that the average division ratio becomes fractional. For example, if an average division ratio of $N + 0.5$ is desired, the divider can alternate between dividing by N and $N + 1$. This simple approach is often referred to as a first-order sigma delta modulator.

However, this straightforward implementation is rarely used in practice for two main reasons. First, the periodic nature of the divider sequence gives rise to strong fractional spurs. Second, the quantization noise is not noise-shaped and therefore appears directly within the PLL bandwidth.

The MASH 1-1 architecture addresses these issues by generating a significantly longer divider sequence while still maintaining the desired average division ratio. Additionally it shapes the quantization noise to higher frequencies. The drawback compared to the first-order SDM implementation is that the timing error now spans two VCO

periods instead of only one, resulting in a larger peak quantization error magnitude.

The MASH 1-1-1 architecture further improves the quantization-noise shaping by pushing a larger portion of the quantization noise toward higher frequencies. The quantization-noise spectra of the MASH 1-1 and MASH 1-1-1 architectures are shown in (5.1) and (5.2), respectively. From these expressions, it can be observed that the MASH 1-1-1 architecture spans four VCO periods, whereas the MASH 1-1 spans only two.

$$\mathcal{L}(f) = 10\log_{10}\left\{\omega_{\text{ref}}^2 \cdot \left(\frac{T_{\text{VCO}}^2}{12}\right)\frac{1}{F_{\text{REF}}} \cdot \left[2\sin(\pi f T_{\text{REF}})\right]^2\right\}\left[\frac{\text{dBc}}{\text{Hz}}\right] \tag{5.1}$$

$$\mathcal{L}(f) = 10\log_{10}\left\{\omega_{\text{ref}}^2 \cdot \left(\frac{T_{\text{VCO}}^2}{12}\right)\frac{1}{F_{\text{REF}}} \cdot \left[2\sin(\pi f T_{\text{REF}})\right]^4\right\}\left[\frac{\text{dBc}}{\text{Hz}}\right] \tag{5.2}$$

A more nuanced description of the sigma delta quantization noise is that the sequence length becomes sufficiently long that the quantization noise is represented by a large number of closely spaced spurs rather than by a truly continuous spectrum, as suggested by (5.1) and (5.2). Nevertheless, these expressions still provide a very accurate approximation of the actual behavior.

If the PLL contains nonlinearities, the shaped quantization noise generated by the MASH 1-1 and MASH 1-1-1 quantization noise can fold into fractional spurs. This phenomenon is analyzed in detail in the next section.

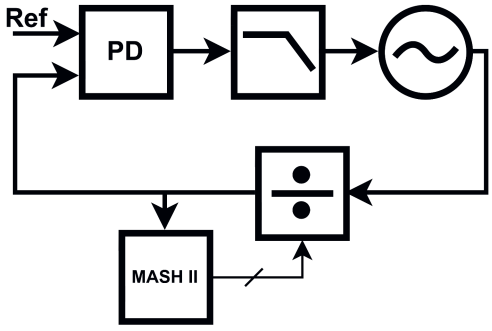


Figure 5.1: Schematic overview of a basic fractional-N PLL.

The architecture shown in Figure 5.1 is rarely used in modern high-performance PLL implementations, as the quantization noise generated by the sigma delta modulation can become significantly larger than the intrinsic phase noise of the oscillator. Instead, more advanced architectures are commonly employed.

An all-digital PLL (ADPLL) is shown in Figure 5.2(a). By employing a time-to-digital converter (TDC), the full phase information becomes directly available in the digital

domain, allowing the loop dynamics and bandwidth to be dynamically adjusted. This enables significantly faster settling behavior and improved programmability. Furthermore, digital implementations generally contain fewer analog building blocks that are sensitive to supply disturbances and substrate coupling. As a result, digital PLLs are often more robust against crosstalk and process variations. In addition, modulation and calibration techniques can be efficiently implemented in the digital domain. Crosstalk-cancellation techniques can also be implemented digitally, and the loop bandwidth can be directly estimated and monitored in the digital domain.

However, these architectures also introduce several challenges. The time-to-digital converter (TDC) often consumes more power than a comparable digital-to-time converter (DTC). An intuitive way to understand this is that a DTC behaves similarly to a DAC, whereas a TDC resembles an ADC. In general, high-performance ADCs are substantially more difficult to design than DACs. Similarly, TDCs typically exhibit larger thermal noise and require careful design to achieve high resolution. In addition, it is considerably more difficult to noise-shape TDC quantization noise, often requiring a larger number of quantization bits and thereby further increasing implementation complexity. Consequently, achieving state-of-the-art phase-noise performance using fully digital PLL architectures remains challenging, particularly in highly phase-noise-sensitive applications.

For these reasons, hybrid PLL architectures are frequently employed, as illustrated in 5.2(b). In these architectures, the fractional modulation is performed similarly to conventional analog PLLs, while a DTC is used to compensate for the quantization noise introduced by the divider modulation. In this way, many of the advantages of digital PLLs can be preserved while avoiding the limitations associated with high-resolution TDCs. Nevertheless, because the full phase error is not directly quantized in the digital domain, the locking behavior is generally somewhat slower compared to fully digital PLLs.

Even so, hybrid PLL architectures still suffer from additional noise sources associated with the interface between the digital and analog domains. These interface circuits can increase both the phase noise and the overall power consumption of the PLL.

The literature generally indicates that analog PLLs assisted by DTCs, such as the architecture shown in 5.2(c), provide some of the best jitter performance and phase-noise-to-power-consumption tradeoffs among modern PLL architectures. For this reason, and due to the demanding requirements discussed in Chapter 2, analog PLLs employing DTC-assisted architectures are considered particularly well suited for highly phase-noise-sensitive applications.

A large number of advanced techniques have been proposed in the literature to further improve the performance of such PLLs. An overview of these approaches is provided in Section 5.4.

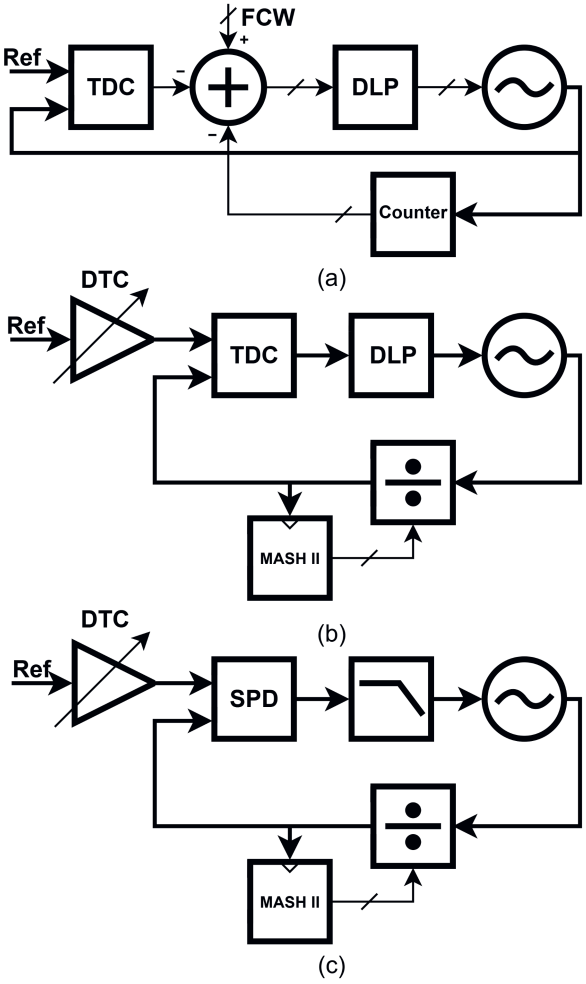


Figure 5.2: Comparison of fractional-N PLL architectures.

5.3 Periodic Nonlinearity Noise theory

In [46], a semi-empirical theory is introduced to analyze the impact of nonlinearities in fractional-N PLLs. This theory is applied here to derive simple expressions for the spurs generated by second and third order nonlinearities. It is assumed in [46] that all nonlinearities are memoryless and can be modeled as a polynomial, as depicted in Figure 5.3, with a nonlinear block NL representing all the nonlinear effects.

The Periodic Nonlinearity Noise (PNN) theory can be understood with reference to

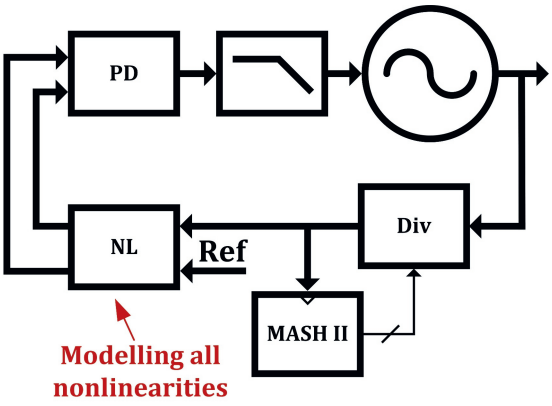


Figure 5.3: Schematic overview of fractional-N PLL, where a block NL has been added to model all nonlinearities.

Figure 5.4. A MASH1-1 SDM introduces a time error that spans two VCO periods. Figure 5.4 (a), illustrates a hypothetical example of nonlinearity (NL), with time error of the input signal on the x-axis, covering two VCO periods. The corresponding NL is on the y-axis, where the nonlinear distortion is also measured in time normalized to a VCO period. Figure 5.4 (b), depicts the two error trajectories, or "traces", that are central to the PNN theory. As shown empirically in [46], a MASH1-1 SDM outputs time errors that alternate between two distinct traces, labeled trace –1 and trace 0. Time progresses along the y-axis in Figure 5.4 (b). At any specific time instant, the time error at the output of the divider is constrained to lie on one of these two traces.

For example, at time τ_1, the time error can either be $-0.8 \cdot \mathrm{T_{VCO}}$ on trace –1 or $+0.2 \cdot \mathrm{T_{VCO}}$ on trace 0 as indicated in Figure 5.4 (b). Similarly, at a later time τ_2, the error is again restricted to one of two values, in this case $-0.6 \cdot \mathrm{T_{VCO}}$ on trace –1 or $+0.4 \cdot \mathrm{T_{VCO}}$ on trace 0. The x-axes in Figure 5.4 (a) and Figure 5.4 (b), correspond to each other and represent the time error at the output of the divider.

The color coding in Figure 5.4 (b), indicates the probability of the system being on trace –1 versus trace 0 as time progresses, where the probability bar to the right goes from zero (blue) to one (red). It is further assumed that the division ratio of the fractional-N PLL is given by (N - a), where N is the integer division value and a is the fractional part. It is well known that spurious tones (spurs) appear at integer multiples of the fractional offset frequency, i.e., at $a \cdot \mathrm{freq_{ref}}$. Consequently, one expects the distortion terms to be periodic with a period of $\mathrm{T_{ref}/a}$, which has been verified empirically in [46]. To reflect this, the y-axis in Figure 5.4 (b), is normalized to $\mathrm{T_{ref}/a}$, so that the value of one on the y-axis corresponds to one fractional period. The PNN itself is described by (5.3). The parameter $\tau_k^{NL}(m)$, as shown in Figure 5.4 (a), represents the nonlinear time deviation associated with each trace k, at normalized time index m, where m is allowed to take values ranging from zero to one, while

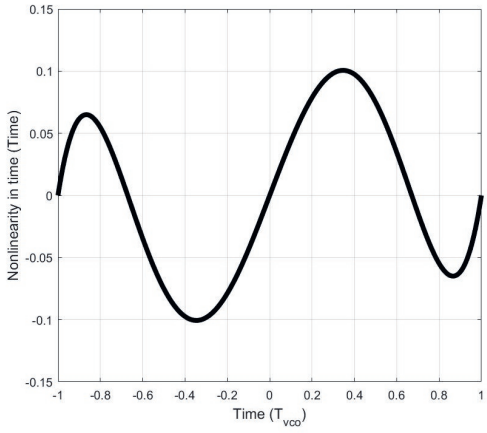


Figure 5.4: Hypothetical nonlinearity (NL) is plotted in time on the y-axis, covering two VCO periods input range (a), and two traces originating from the SDM where the error at the output of the divider is shown on the x-axis, normalized to a VCO period, and the y-axis is normalized to one fractional period, Tref /a. The traces are color-coded, with the bar on the right indicating the probability of being on trace –1 or trace 0 as it changes over time (b).

$P\left(\tau_k^{NL}(m)\right)$ represents the probability for being at the two trace respectively. The PNN can be interpreted as the distortion term and has the unit of time. Notably, this formulation differs slightly from that in [46], where the index m took on discrete values 1, 2,. . . , 1/a. The normalization adopted here, where m instead ranges from 0 to 1, is chosen to simplify the mathematical expressions. Furthermore, the probabilities of a MASH1-1 being on trace -1 or trace 0 are given by (5.4) and (5.5), respectively, as established in [47].

$$PNN(m) = \sum_{k=-1}^{0} \tau_k^{NL}(m)\, P\left(\tau_k^{NL}(m)\right) \tag{5.3}$$

$$Trace\ -1: \qquad P\left(\tau_k^{NL}(m)\right) = m \tag{5.4}$$

$$Trace\ 0: \qquad P\left(\tau_k^{NL}(m)\right) = 1 - m \tag{5.5}$$

The error or time deviation introduced by a MASH1-1 SDM at the divider output spans across two VCO periods. A hypothetical quadratic nonlinearity is described by (5.6), where t_e is the time error at the output of the divider normalized to one VCO period and plotted over the corresponding signal range in Figure 5.5 (a). As can be seen A_{NL2} represents the maximum time deviation in the range. The x-axis is normalized with respect to the VCO period. From (5.3) and (5.6), the nonlinear time deviations $\tau_{k=-1}^{NL}$ and $\tau_{k=0}^{NL}$ can be derived, as shown in (5.7) and (5.8), respectively, where the variable m ranges from 0 to 1. By applying (5.3), (5.4), (5.5), (5.7), and (5.8), the resulting $PNN(m)$ function can be calculated, as shown in (5.9). The $PNN(m)$ function must have zero mean; therefore, the constant term $\frac{5}{6}A_{NL2}$ is added to ensure this condition is met. Performing a Fourier series expansion of (5.9) yields (5.10), from which the harmonic content of $PNN(m)$ becomes clearly observable. In (5.10), n denotes the order of the Fourier coefficients. The resulting $PNN(m)$ is illustrated in Figure 5.5(b), where the x-axis is normalized by T_{ref}/a, with T_{ref} denoting the reference clock period and a denoting the fractional division control word.

$$\tau_{NL}(t_e) = -A_{NL2}(t_e + 1)(t_e - 1) \tag{5.6}$$

$$\tau^{NL}_{k=-1}(m) = -A_{NL2}m(m - 2) \tag{5.7}$$

$$\tau^{NL}_{k=0}(m) = -A_{NL2}(m + 1)(m - 1) \tag{5.8}$$

$$PNN(m) = -A_{NL2}\left(m^2 - m + 1\right) + \frac{5}{6}A_{NL2} \tag{5.9}$$

$$PNN(m) = \sum_{n=1}^{\infty} \frac{-A_{NL2}}{\pi^2 n^2} \cos(2\pi nm) \tag{5.10}$$

A similar calculation can be carried out for the third order nonlinearity as well. The non-linearity for a third order distortion is given by (5.11), which is normalized such that A_{NL3} represents the maximum deviation in time for the third order distortion. Where t_e is the time error normalized to one VCO period. This is illustrated in Figure 5.6(a). The trace probability remains the same as in the case of the second order nonlinearity, as expressed by (5.4) and (5.5). From (5.3), (5.4), (5.5) and (5.11), the nonlinear time deviations $\tau^{NL}_{k=-1}$ and $\tau^{NL}_{k=0}$ can be derived, as shown in (5.12) and (5.13) for the third order nonlinearity, where the variable m ranges from 0 to 1. The resulting PNN(m) function can then be calculated, as (5.14). Performing a Fourier series expansion of (5.14) yields (5.15). In (5.15), n is the order of the Fourier coefficients. The resulting PNN(m) in (5.14) is illustrated in Figure 5.6(b), where the x-axis is normalized by T_{ref}, with T_{ref}/a denoting the reference clock period and a representing the fractional division control word.

$$\tau_{NL}(t_e) = A_{NL3}\sqrt{\frac{27}{4}}\,(t_e - 1)t_e(t_e + 1) \tag{5.11}$$

$$\tau^{NL}_{k=-1}(m) = A_{NL3}\sqrt{\frac{27}{4}}\,(m - 2)(m - 1)m \tag{5.12}$$

$$\tau^{NL}_{k=0}(m) = A_{NL3}\sqrt{\frac{27}{4}}\,(m - 1)m(m + 1) \tag{5.13}$$

$$PNN(m) = -A_{NL3}\sqrt{\frac{27}{4}}\,\left(2m^3 - 3m^2 + m\right) \tag{5.14}$$

$$PNN(m) = \sqrt{\frac{27}{4}}\sum_{n=1}^{\infty} \frac{-3A_{NL3}}{\pi^3 n^3} \sin(2\pi nm) \tag{5.15}$$

Based on (5.10) and (5.15), the spurious tones of the PLLs can be calculated. A

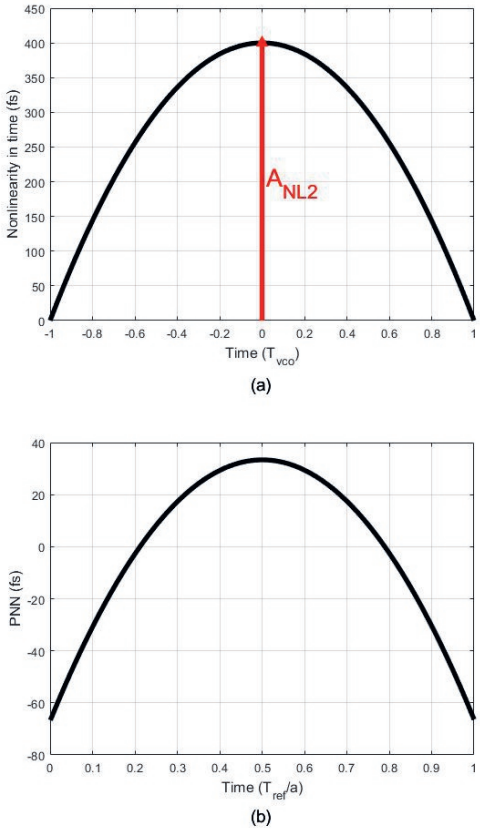


Figure 5.5: Quadratic nonlinearity, where A_{NL2} indicate maximum time error deviation (a), and accompanying PNN for a MASH1-1 SDM (b).

straightforward formula for determining the magnitude of the first and most significant spur, located at the fractional frequency offset a·freqref from the carrier, can be derived for a second order nonlinearity as shown in (5.16). This requires only the maximum time deviation of the second order nonlinearity and the output frequency of the PLL (oscillation frequency of the output oscillator to be known). Similarly, a simple formula for the third order nonlinearity can be derived in (5.17). These formulas can be easily modified to calculate the magnitude of higher order spurs, by taking the higher order Fourier coefficients in (5.10) and (5.15).

$$Spur_{dBc} = 20\log\left(2\pi f_{\text{req,osc}}\left(\frac{A_{NL2}}{2\pi^2}\right)\right) \tag{5.16}$$

$$Spur_{dBc} = 20\log\left(2\pi f_{\text{req,osc}}\sqrt{\frac{27}{4}}\left(\frac{3A_{NL3}}{2\pi^3}\right)\right) \tag{5.17}$$

$$A_{NL} = \sqrt{\left(\frac{A_{NL2}}{2\pi^2}\right)^2 + \left(\sqrt{\frac{27}{4}}\left(\frac{3A_{NL3}}{2\pi^3}\right)\right)^2} \tag{5.18}$$

$$Spur_{dBc} = 20\log(2\pi f_{\text{req,osc}} A_{NL}) \tag{5.19}$$

As can be seen in (5.10) and (5.15), there is a 90-degree phase difference between the PNN components for the second order and third order nonlinearities. Consequently, the spur magnitudes cannot be added directly, to get the result of the combined second and third order nonlinearity, but they must instead be combined in power as described by (5.18) and (5.19). The analytical expressions in (5.16) and (5.17) are verified using a MATLAB simulation. In Figure 5.7, a MASH1-1 SDM signal is passed through a second order nonlinearity, where the nonlinearity coefficient A_{NL2} is 400 fs (as in Figure 5.4 (a)). The oscillator frequency is 100 MHz, and the fractional frequency division ratio is 0.0038. Similarly, in Figure 5.8, the spur due to a third order nonlinearity (shown in Figure 5.6 (a)) is plotted, with $A_{NL3} = 200$ fs. Substituting these values into (5.16) and (5.17) and confirms that the calculated spur levels are within 0.1 dB of those predicted by the analytical expressions. Finally, it is important to note that the formulas for spur estimation (5.16), (5.17), and (5.19) assume that the spurs are located within the PLL bandwidth, such that the loop filter does not suppress them. These formulas can be readily modified to account for the attenuation effects of the PLL loop filter when the spurs fall outside the PLL's bandwidth. This paper specifically addresses the MASH1-1 SDM, which exhibits a time error spanning only two VCO periods at the output of the divider. Unlike higher order SDMs such as MASH1-1-1, the lower time error introduced by MASH1-1 results in reduced quantization and thermal noise. However, the analysis presented here can be straightforwardly extended to higher order SDM, such as the MASH1-1-1 and the broader family of ENOP-based SDM [48].

5.4 State of the art

Nonlinearity in the circuits responsible for addressing sigma-delta quantization noise such as DTCs, phase interpolators and TDCs can lead to noise folding and the introduction of significant in-band spurs. This issue has been widely recognized, and substantial research efforts have been dedicated to mitigating its impact. Broadly, these approaches fall into four categories: digital predistortion, analog techniques such as

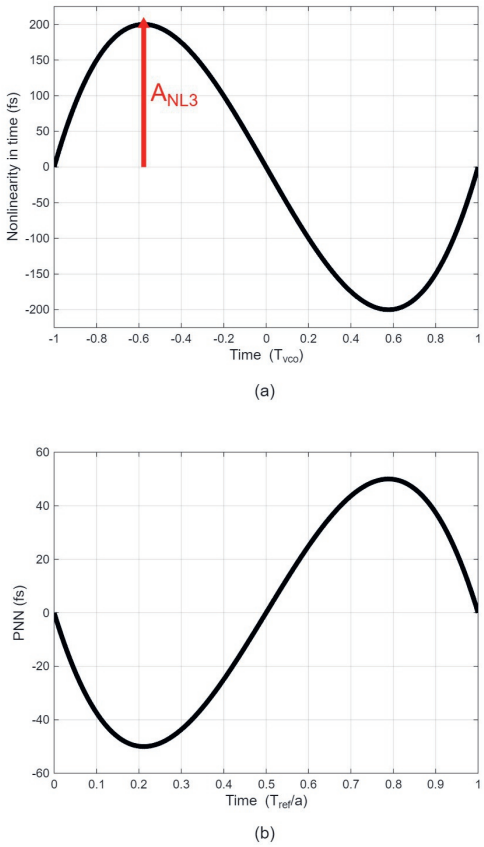


Figure 5.6: Third order nonlinearity, where A_{NL3} indicate maximum time error deviation (a), and accompanying PNN for MASH1-1 SDM (b).

pseudo differential DTCs and constant slope DTCs, dithering techniques and higher order more sophisticated SDM, and cascaded PLLs. Digital predistortion techniques often require long convergence times for calibration of coefficients and can complicate verification [49], [50], [51]. Dithering methods, both subtractive [52], [53] and non-subtractive [51] can effectively suppress spurious tones, but they do so at the cost of increased quantization and thermal noise, as they expand the magnitude of the signal time difference input to the phase detector. The family of enhanced nonlinearity-induced noise performance reduction techniques (ENOP) [48] shares similarities with non-subtractive dithering and suffers from similar trade-offs in terms of noise and

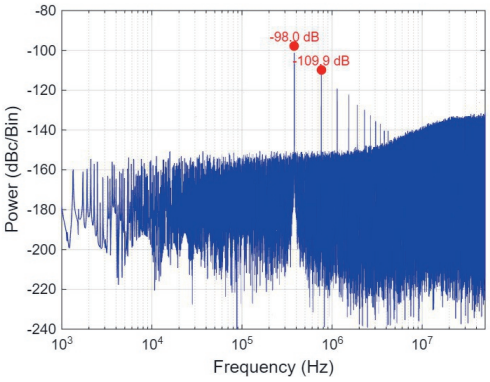


Figure 5.7: Time domain simulation of spur magnitude with second order nonlinearity, where A_{NL2} is 400 fs, the oscillator frequency is set to 100 MHz and the fractional frequency control word is 0.0038.

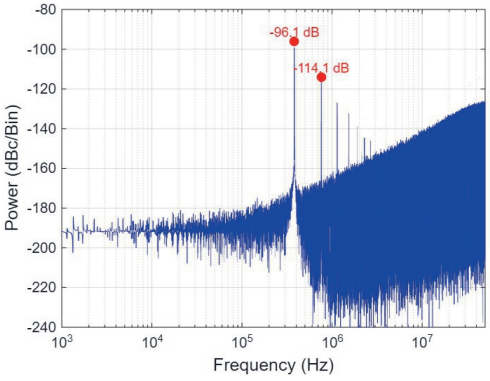


Figure 5.8: Time domain simulation of spur magnitude with third order nonlinearity, where A_{NL3} is 200 fs, the oscillator frequency is set to 100 MHz and the fractional frequency control word is 0.0038.

power performance. Analog approaches such as constant slope DTCs [54] and the improved iteration, inverse constant slope DTCs [52], [55], offer improved linearity compared to variable slope DTCs but often come with degraded noise power tradeoffs in comparison to variable slope DTCs [56]. Cascaded PLL architectures can achieve excellent spur suppression without complicated calibration schemes [57], [58]. However, the use of multiple VCOs introduces challenges, due to increased chip area and oscillator coupling which can result in relatively large spurs [57], [11]. The phase selector schemes in [59], [60] lower power consumption and reduce spurs, but come at the cost of additional calibration. Design guidelines for a linear phase detector

are discussed extensively in [61]. However, this approach does not suppress SDM quantization noise. In [62], [63] a linearization scheme is proposed that uses several SDMs operated in parallel with different time offset between them. In addition to providing suppression of fractional spurs, it has the advantage of not expanding the time error at the input of the phase detector, and it also suppresses quantization noise. The next section analyses the linearization approach in [62], [63] further, building on the analytical framework in [63], deriving closed-form formulas for the suppression of fractional spurs in the case of second and third order nonlinearities and analyses the effect of phase rotation on the linearization performance, the results are validated by MATLAB simulations.

5.5 Analysis of Parallel SDM With Time Offsets

The basic idea in [62], [63] is to operate several MASH1-1 SDMs in parallel, each with a different time offset relative to the others, as shown in Figure 5.9. And thereby change the periodicity of the PNN function and suppress it peak magnitude. The modulators can be easily run with time offsets by initializing their starting values differently. When an SDM is operated with a time offset corresponding to m = 0.5, its SDM code pattern is shifted by half a fractional period. In addition, the output signal of the frequency divider controlled by the SDM experiences a time shift equivalent to half a period of the VCO. It's the case that even if the SDM sequence is shifted with half a fractional period, the signal from the divider only experiences 0.5 VCO period time shift.

The half VCO period shift of the divider output signal can be compensated for by applying a phase shift (time shift) $\Delta\phi$, as illustrated in Figure 5.9. Alternatively, the phase detectors can be operated with DC offsets, where one detector produces an output signal with positive DC and the other produces a negative DC output. These signals are then summed to the correct overall DC level at the output of the phase detectors. Furthermore, it will be shown that the effectiveness of the linearization techniques differs significantly between even and odd order nonlinearities, depending on whether the divider signals phase shift is compensated or not. Even order distortion can be effectively suppressed even in the absence of phase shift compensation, but for odd order nonlinearities, compensating for the phase shift is essential for the linearization techniques to remain effective. For this reason, even and odd order nonlinearities are treated separately in the analysis.

5.5.1 Even Order Nonlinearity

First, it is assumed that the phase shifts are perfectly compensated by applying a phase adjustment $\Delta\phi$, as illustrated in Figure 5.9. In Figure 5.10, the red curve illustrates the $PNN(m)$ from Figure 5.5(a), originating from a second-order quadratic nonlinearity with a maximum deviation of 400 fs. The blue curve represents a $PNN(m)$ with the same nonlinearity, but with the SDM time offset by half a fractional period. Finally, the black curve shows the summation of the two different $PNN(m)$ functions,

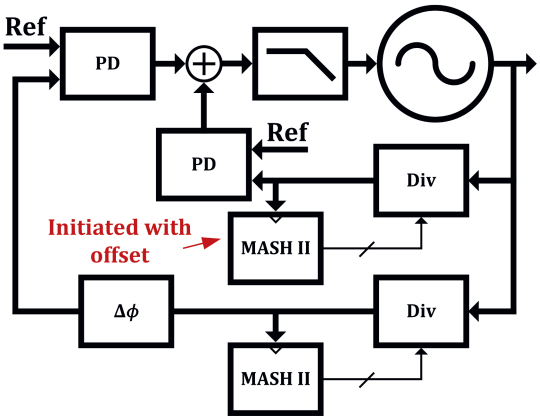


Figure 5.9: Proposed linearization scheme. Two SDMs are operated in parallel with time offset. Their quantization errors (noise) are added together after the phase detectors.

resulting in (5.20). By substituting (5.10) into (5.20) and simplifying the result, (5.21) is obtained. As can be seen, the odd-order components of the spurious signals are fully suppressed, and the first spur appears at twice the fractional frequency, $2a \cdot f_{\text{req,ref}}$. In Figure 5.11, the Fourier coefficients of the red and black $PNN(m)$ curves from Figure 5.10 are plotted. It is clear that the odd-order frequency components have been effectively canceled by the summation. As can be seen in (5.21), both the cosine term and the denominator now contain $2n$ instead of n, indicating that the amplitude is suppressed and the period is halved, as expected from Figure 5.10. From (5.21), it can be calculated that the scheme suppresses the most significant spur by approximately 12 dB, which is now located at twice the fractional frequency, i.e., $2a \cdot f_{\text{req,ref}}$.

The theory developed here is verified using a time-domain simulation in MATLAB. As in the previous simulation, the oscillator frequency is assumed to be 100 MHz, and the fractional frequency control word is 0.0038. In this setup, two SDMs are operated with a half-fractional-period offset corresponding to $m = 0.5$. The output error signals from the SDMs pass through a quadratic nonlinearity with $A_{NL2} = 400$ fs and are then summed. The spectrum of the resulting signal is shown in Figure 5.12. Comparing Figure 5.7 with Figure 5.12, it is clearly observed that the even-order spurs remain unaffected, while the odd-order spurs are eliminated. This confirms the validity of the $PNN(m)$ framework for analyzing the superposition of SDMs.

$$PNN_{sum}(m) = \frac{1}{2}PNN_{NL2}(m) + \frac{1}{2}PNN_{NL2}\left(m + \frac{1}{2}\right) \tag{5.20}$$

$$PNN_{sum}(m) = \sum_{n=1}^{\infty} \frac{A_{NL2}}{\pi^2(2n)^2} \cos(2\pi(2n)m) \tag{5.21}$$

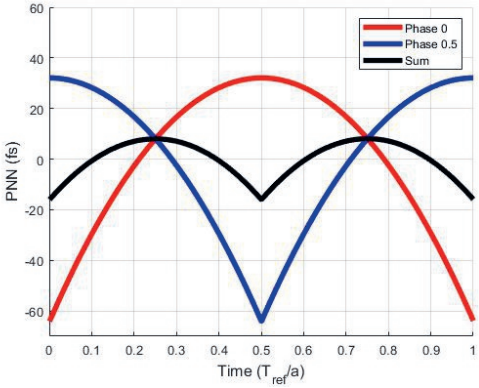


Figure 5.10: Red curve, PNN for a quadratic nonlinearity with ANL2 = 400 fs. Blue curve: PNN when the SDM is operated with 0.5 fractional period time offset. Black curve: the sum of the two PNN components, as described by (5.20).

It is possible to operate more than two MASH1-1 SDMs in parallel. For example, if four MASH1-1 SDMs are operated with relative offsets of 0, 0.25, 0.5, and 0.75, the largest spur is reduced by approximately 24 dB compared to the case where a single SDM is used. More generally, if N SDMs are operated in parallel with uniform offsets of 0, $1/N$, ..., $(N-1)/N$, and the phase shift is perfectly compensated, the resulting $PNN(m)$ function is given by Figure 5.13. In this configuration, the first and most significant spur appears at N times the fractional frequency, i.e., $N \cdot a \cdot f_{\text{req,ref}}$. This result is consistent with the analytical analysis presented in [63], but is derived here using the $PNN(m)$ framework. Additionally, the spur suppression scales as $20 \cdot \log(N^2)$. For instance, operating 16 SDMs in this manner yields a suppression of the largest spur by approximately 48 dB.

$$PNN_{sum}(m) = \sum_{n=1}^{\infty} \frac{A_{NL2}}{\pi^2(Nn)^2} \cos(2\pi(Nn)m) \tag{5.22}$$

In [62], [63] the time offset between the SDM paths is compensated using an auxiliary DTC and additional calibration. This approach lends itself naturally to digital

PLLs. While similar techniques can be applied to analog PLLs [64], they result in substantially higher overhead, particularly when many SDMs are used. In contrast, two phases with 0.5 VCO-period offsets can easily be generated using a differential oscillator, and four phases are readily obtainable from a quadrature oscillator.

For this reason, it is important to study the effect of the linearization technique also in the absence of phase compensation. As discussed earlier, when two SDMs are operated with a half-fractional-period time offset, their corresponding divider output signals exhibit a relative phase shift of half a VCO period. When the PLL is locked, this results in one phase detector indicating a positive average time error of $T_{\mathrm{VCO}}/4$, while the other indicates an average negative time error of $-T_{\mathrm{VCO}}/4$.

The impact of this on the linearization effect can be understood with reference to Figure 5.13. In Figure 5.13, a quadratic nonlinearity spanning 2.5 VCO periods is shown, reflecting the fact that the two feedback signals have a half-VCO-period offset. Figure 5.13(b) displays the trace of the SDM time offset, shifted forward by half a fractional period, while Figure 5.13(c) shows the trace of the original, non-offset SDM. Due to the difference in mean time error at the phase detectors, the traces are shifted in opposite directions and are separated by half a VCO period, as illustrated in Figure 5.13.

The central question is whether the behavior observed in Figure 5.10 is preserved despite the relative phase shift of the divider signals. This is the case if the $PNN(m)$ of the offset SDM is identical to the $PNN(m)$ of the original SDM, except for a 0.5 time shift. In Figure 5.13(b) and (c), this can be observed at the times τ_1 and τ_2, where the $PNN(m)$ in Figure 5.13(b) at time τ_2 equals the $PNN(m)$ in Figure 5.13(c) at time τ_1, with τ_1 and τ_2 differing by 0.5 fractional periods.

Furthermore, the $PNN(m)$ can be derived explicitly by assuming the nonlinearity given in Eq. (5.23), which highlights that the two SDMs cover 2.5 VCO periods due to the carrier phase shift.

$$\tau_{NL}(t_e) = -A_{NL2}(t_e + 1.25)(t_e - 1.25) \tag{5.23}$$

The $PNN(m)$ function for the combined offset SDMs can be calculated using Eqs. (5.24) and (5.25) for the ranges $0 < m < 0.5$ and $0.5 < m < 1$, respectively.

$$PNN(m) = -A_{NL2}\left(m^2 - 0.5m\right) - \frac{1}{24}A_{NL2}, \qquad 0 < m < 0.5 \tag{5.24}$$

$$PNN(m) = -A_{NL2}\left(m^2 - 1.5m\right) - \frac{13}{24}A_{NL2}, \qquad 0.5 < m < 1 \tag{5.25}$$

A careful examination of these equations shows that the PNN expression in (5.25) is a time shifted version of (5.24) by 0.5, confirming that the overall behavior remains

unchanged even without compensating for the carrier phase shift. This holds true despite the signal now spanning a range that is 0.5 VCO periods wider.

The fact that the two SDMs cover 2.5 VCO periods in the uncompensated case result in the peak time error being somewhat larger, in this case 625 fs instead of 400 fs, as can be seen in Figure 5.13(a), but importantly, the nonlinearity remains unchanged; in (5.23), (5.24), and (5.25), the coefficient of the m2, ANL2, is still 400 fs. When the divider output signal time shift is left uncompensated, it is reasonable to ask whether exciting a broader portion of the nonlinearity leads to an amplification of the spur at twice the fractional frequency. Taking the Fourier transform of (5.24) and (5.26) for m ranging from zero to one, results in (5.24). However, (5.26) is just the same equation as (5.21), the compensated case, meaning that all the properties of the compensated case are still valid for the uncompensated case, for a quadratic nonlinearity with two SDMs.

$$PNN_{sum}(m) = \sum_{n=1}^{\infty} \frac{A_{NL2}}{\pi^2(2n)^2} \cos(2\pi(2n)m) \tag{5.26}$$

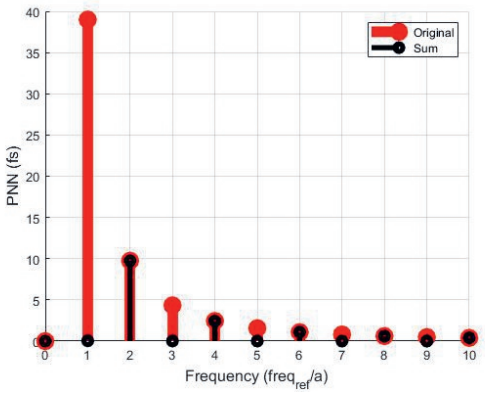


Figure 5.11: Red curve: Fourier coefficient of the original PNNs for quadratic nonlinearity as shown in red in Figure 5.10. Black curve: shows the Fourier coefficient for the PNN of the sum of the two SDMs, as shown in black in Figure 5.10.

In the case where four SDMs operate with time offsets of 0, 0.25, 0.5, and 0.75, the scenario is analyzed below. It is assumed that the phase shift is left uncompensated. Due to this, the time error spans 2.75 VCO periods. The NL is defined in (5.27), where the peak value of the NL here is 756 fs. The PNN is derived in (5.28), (5.29), (5.30), and (5.31). It has a periodicity of 0.25, which ensures that the spurs at fractional frequency orders one, two and three are eliminated, even without carrier phase compensation in this case.

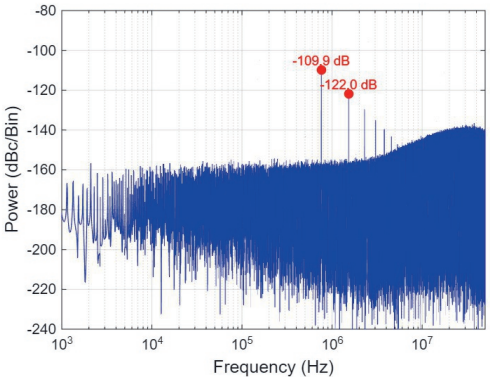


Figure 5.12: Fourier transform of time domain simulation of two MASH1-1 SDM operated with 0.5 fractional period time offset, otherwise using same scenario as in Figure 5.7.

$$\tau_{NL}(t_e) = -A_{NL2}(t_e + 1.375)(t_e - 1.375) \tag{5.27}$$

$$PNN(m) = -A_{NL2}\left(m^2 - \frac{1}{4}m\right) - \frac{1}{96}A_{NL2}, \qquad 0 < m < 0.25 \tag{5.28}$$

$$PNN(m) = -A_{NL2}\left(m^2 - \frac{3}{4}m\right) - \frac{13}{96}A_{NL2}, \qquad 0.25 < m < 0.5 \tag{5.29}$$

$$PNN(m) = -A_{NL2}\left(m^2 - \frac{5}{4}m\right) - \frac{37}{96}A_{NL2}, \qquad 0.5 < m < 0.75 \tag{5.30}$$

$$PNN(m) = -A_{NL2}\left(m^2 - \frac{7}{4}m\right) - \frac{73}{96}A_{NL2}, \qquad 0.75 < m < 1 \tag{5.31}$$

5.5.2 Odd Order Nonlinearity

Similarly, formulas for third-order nonlinearity can be derived. First, it is assumed that the phase shift is compensated for. In (5.32), the spurious tones are calculated for two MASH 1-1 SDMs operating out of phase under a third-order nonlinearity, resulting in an 18 dB suppression compared to the standard case in (5.15). When four MASH 1-1 SDM modulators are used in parallel, a 36 dB suppression is achieved relative to the standard SDM configuration in (5.15).

More generally, if N SDMs are operated in parallel with uniform offsets of

$$0, \ \frac{1}{N}, \ \ldots, \ \frac{N-1}{N}$$

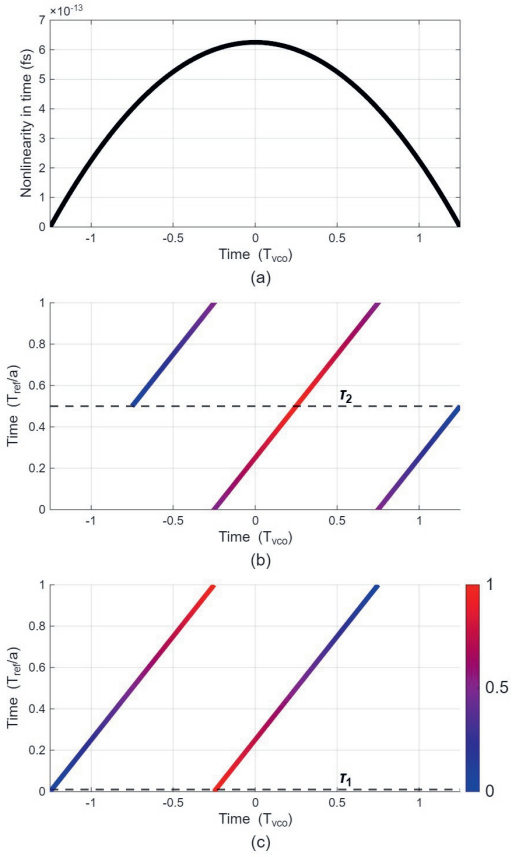


Figure 5.13: Proposed linearization scheme. Two SDMs are operated in parallel with time offset. Their quantization errors (noise) are added together after the phase detectors.

and the carrier signals are perfectly phase compensated, the resulting PNN function is given by (5.33). In this configuration, the first and most significant spur appears at N times the fractional frequency, i.e., $N \cdot \alpha \cdot f_{\text{ref}}$. Additionally, the spur suppression scales as $20\log(N^3)$.

$$\mathrm{PNN}(m) = \sqrt{\frac{27}{4}} \sum_{n=1}^{\infty} \frac{3A_{\mathrm{NL3}}}{\pi^3 (2n)^3} \sin(2\pi(2n)m) \tag{5.32}$$

$$\mathrm{PNN}(m) = \sqrt{\frac{27}{4}} \sum_{n=1}^{\infty} \frac{3A_{\mathrm{NL3}}}{\pi^3 (Nn)^3} \sin(2\pi(Nn)m) \tag{5.33}$$

However, due to the odd symmetry of the odd-order nonlinearity, where

$$\tau_{\mathrm{NL}}(m) = -\tau_{\mathrm{NL}}(-m),$$

the suppression is significantly reduced in cases where the phase shift is left uncompensated. As the SDMs now span 2.5 VCO periods, the same nonlinearity can be expressed as in (5.34). This is the same expression as in (5.11), except that the zero end points have been moved from ± 1 to ± 1.25 to accommodate the wider range.

It is important to note that the cubic nonlinear coefficient, A_{NL3}, remains the same in both (5.11) and (5.34) for the same system nonlinearity. The PNN can then be calculated as shown in (5.35) and (5.36).

$$\tau_{\mathrm{NL}}(t_e) = A_{\mathrm{NL3}} \sqrt{\frac{27}{4}} (t_e - 1.25) t_e (t_e + 1.25) \tag{5.34}$$

$$\mathrm{PNN}_{\mathrm{sum}}(m) = A_{\mathrm{NL3}} \sqrt{\frac{27}{4}} \left(2m^3 - \frac{3}{2}m^2 + \frac{5}{8}m - \frac{3}{32} \right), \qquad 0 < m < 0.5 \tag{5.35}$$

$$\mathrm{PNN}_{\mathrm{sum}}(m) = A_{\mathrm{NL3}} \sqrt{\frac{27}{4}} \left(2m^3 - \frac{9}{2}m^2 + \frac{23}{8}m - \frac{15}{32} \right), \qquad 0.5 < m < 1.0 \tag{5.36}$$

In Figure 5.14, the red curve shows the PNN for a third-order nonlinearity with $A_{\mathrm{NL3}} = 200$ fs, which is the same value used in Figure 5.6(b). The black curve represents the sum of the original PNN and a version phase shifted by 0.5, corresponding to the case where the carrier phase shift has not been compensated. The blue curve shows the summation of the original red curve and a curve phase shifted by 0.5, but in this case the divider phase shift (time shift) has been compensated for.

The Fourier series coefficients of the black and red curves are shown in Figure 5.15. The first Fourier coefficient, representing the most significant spur located at the first fractional frequency, has been suppressed from approximately 50 fs to 40 fs, corresponding to only 1.9 dB. This demonstrates that, for third-order nonlinearities, the linearization provides only a minor improvement in the absence of divider signal phase compensation.

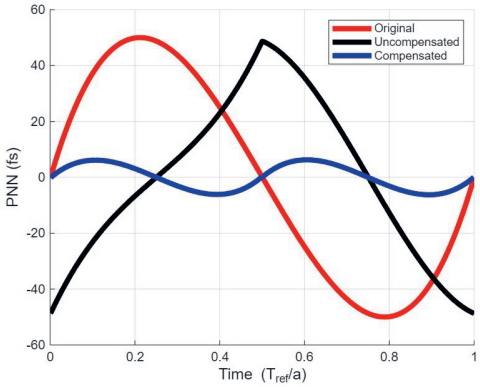


Figure 5.14: Red curve: PNN for a third order nonlinearity with $A_{\mathrm{NL3}} = 200$ fs (same as in Figure 5.6(b)). Black curve: PNN for sum of the time shifted SDM, where the phase shift have been compensated for. Blue curve: same as black, but with phase shift compensation.

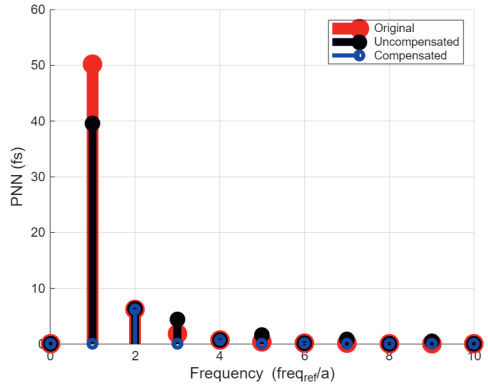


Figure 5.15: Red curve: Fourier coefficient of the original red PNNs for third order nonlinearity PNN shown in Figure 5.14. Black curve: Fourier coefficients of the PNN of the sum of two SDMs, as plotted in black (Uncompensated) in Figure 5.14.

5.5.3 Mismatch Analysis

The analytical expressions derived thus far are valid under the assumption of ideal, perfectly matched paths. In practical implementations, however, several sources of circuit impairments can degrade the effectiveness of the proposed linearization technique. Three primary mechanisms can be identified. First, differences in routing lengths among the parallel signal paths can introduce relative phase shifts. Second,

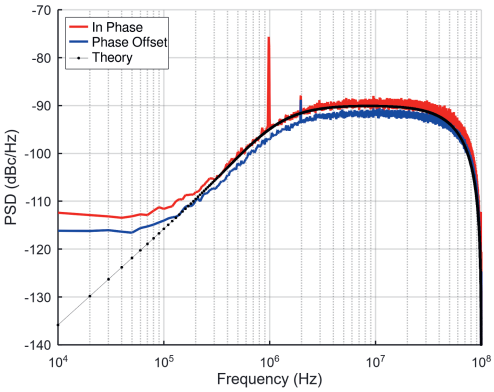


Figure 5.16: Red curve: PSD from quantization noise of two SDMs in phase. Blue curve: PSD from two SDMs with half a period offset. Black curve: Theoretically calculated curve for the red case.

random phase deviations originating from, for example, random mismatches in divider delay time can further impair the linearization technique. These phase discrepancies particularly affect the suppression of odd-order nonlinearities, as the effective cancellation of these relies on precise phase alignment. Third, gain mismatches in the phase detector or associated analog paths can prevent full cancellation of distortion components.

In contrast, the suppression of second-order nonlinearities is less sensitive to phase mismatch. Routing length differences have negligible effect, and only gain mismatch in the phase detection path significantly influences the residual second-order spur levels. The residual $\mathrm{PNN}_{\mathrm{miss}}(m)$ caused by phase-detector mismatch is given by (5.37), where K_{PD1} and K_{PD2} denote the gains of phase detector one and two, respectively. It is important to note that the analytical expressions are valid only when referred to the input of the phase detector. Accordingly, in (5.37), the PNN is input referred by normalizing with respect to the combined gain of both phase-detector paths. This ensures that the derived results accurately reflect the behavior of the system at the point where the nonlinearity is introduced and observed. The PNN in (5.37) can then be used in combination with (5.26) to predict the magnitude and location of all spurs for known properties of phase-detector mismatch and quadratic nonlinearity.

$$\mathrm{PNN}_{\mathrm{miss}}(m) = \frac{(K_{\mathrm{PD1}} - K_{\mathrm{PD2}})}{(K_{\mathrm{PD1}} + K_{\mathrm{PD2}})} \frac{A_{\mathrm{NL2}}}{\pi^2} \cos(2\pi m) \tag{5.37}$$

The situation for odd-order nonlinearities is more complex. In this case, phase mismatches arising from imperfect phase-shift compensation, differences in routing lengths, and gain mismatches between the phase-detector paths collectively re-

duce the achievable spur suppression. These impairments limit the effectiveness of the linearization technique for odd-order terms. The residual spur level caused by phase-detector gain mismatch in the presence of third-order nonlinearity is expressed in (5.38), which is analogous in form to the second-order case presented in (5.37).

$$\mathrm{PNN}_{\mathrm{miss}}(m) = \frac{(K_{\mathrm{PD1}} - K_{\mathrm{PD2}})}{(K_{\mathrm{PD1}} + K_{\mathrm{PD2}})} \sqrt{\frac{27}{4}} \frac{3A_{\mathrm{NL3}}}{\pi^3} \sin(2\pi m) \tag{5.38}$$

The effect of imperfect phase compensation is studied for the case where the SDMs operate with a 0.5 fractional-period time difference. The carrier phase shift is imperfectly compensated, leaving a residual phase difference of $2\Delta\phi$. The nonlinearity is therefore defined as

$$\tau_{\mathrm{NL}}(m) = A_{\mathrm{NL3}} \sqrt{\frac{27}{4}} (m - 1 - \Delta\phi) m (m + 1 + \Delta\phi) \tag{5.39}$$

The resulting PNN can then be derived as

$$\mathrm{PNN}_{\mathrm{sum}}(m) = A_{\mathrm{NL3}} \sqrt{\frac{27}{4}} \left(2m^3 - \frac{3}{2}m^2 + \left(\frac{1}{4} + \frac{3}{2}\Delta\phi \right) m - \frac{3}{8}\Delta\phi \right), \qquad 0 < m < 0.5 \tag{5.40}$$

$$\mathrm{PNN}_{\mathrm{sum}}(m) = A_{\mathrm{NL3}} \sqrt{\frac{27}{4}} \left(2m^3 - \frac{9}{2}m^2 - \left(\frac{3}{2}\Delta\phi - \frac{13}{4} \right) m + \left(\frac{9}{8}\Delta\phi - \frac{3}{4} \right) \right), \qquad 0.5 < m < 1 \tag{5.41}$$

The first term in the Fourier-series expansion of (5.40) and (5.41) is given by

$$\mathrm{PNN}_{\mathrm{miss}}(m) = \frac{\Delta\phi}{12\pi^2} \sqrt{\frac{27}{4}} \frac{3A_{\mathrm{NL3}}}{\pi^3} \cos(2\pi m) \tag{5.42}$$

The resulting PNN caused by phase-detector gain mismatch and phase mismatch for third-order nonlinearities exhibits a 90° phase difference. To accurately determine the amplitude of the first fractional spur originating from both effects, they can therefore be combined as

$$A_{\mathrm{NL}} = \sqrt{\frac{27}{4}} \frac{3A_{\mathrm{NL3}}}{\pi^3} \sqrt{\left(\frac{\Delta\phi}{6\pi^2} \right)^2 + \left(\frac{K_{\mathrm{PD1}} - K_{\mathrm{PD2}}}{K_{\mathrm{PD1}} + K_{\mathrm{PD2}}} \right)^2} \tag{5.43}$$

$$\mathrm{Spur}_{\mathrm{dBc}} = 20 \log(2\pi f_{\mathrm{req_{osc}}} A_{\mathrm{NL}}) \tag{5.44}$$

Assuming a phase-detector mismatch of one percent, i.e.,

$$\Delta K_{\mathrm{PD}} = 0.01,$$

and a divider time-compensation mismatch corresponding to five percent of a VCO period,

$$\Delta\phi = 0.05,$$

then (5.43) shows that the spur located at the first fractional offset frequency is not eliminated but suppressed by approximately 40 dB compared to the case where only a single SDM is used.

5.5.4 Quantization Noise

The architecture offers two key advantages. First, it effectively suppresses spurious tones, and second, it reduces the SDM modulator quantization noise. To analyze the effect this scheme has on quantization noise, a closed-loop simulation was carried out in MATLAB using the following parameters. The reference frequency was equal to 100 MHz, and the divider ratio was 80, resulting in an output frequency of 8 GHz. The charge-pump current I_{CP} was set to 0.5 mA for each of two branches, so that they combined provide a total of 1 mA. The low-pass filter capacitor was chosen to be 65 pF, and the resistor was set to 5 kΩ. The K_{VCO} was 200 MHz/V. This results in a PLL with a bandwidth of approximately 1 MHz. A large quadratic nonlinearity of $A_{\mathrm{NL2}} = 5$ ps was added, and it was further assumed that the time offset is perfectly compensated for.

The simulation was carried out for a fractional control word of 0.00938, and the result is plotted in Figure 5.16 for the case when the SDMs are in phase (red) and the case when the SDMs are driven with an offset corresponding to half a fractional period (blue). Welch's method was used to estimate the power spectral density (PSD), averaged 400 times. The black curve is the theoretically calculated curve for the case where the SDMs are operated without offset and shows close agreement with the simulation. The deviation from the theoretical curve (black) at low frequencies is due to the large nonlinearity added to the model.

As experimentally verified in [62], [63], and further verified here by simulation, the first spur is eliminated while the second spur remains unchanged. The small change observed in the amplitude of the second spur is due to the lower quantization noise in the case of the blue curve. If the time-offset SDM signals were completely uncorrelated, a 3 dB reduction in quantization noise would be expected, as shown in [25], where uncorrelated white noise applied to three DTCs operating in parallel results in a 4.8 dB phase-noise improvement. However, a close inspection of Figure 5.16 reveals only a 2 dB reduction. This suggests that the quantization noise from the different MASH 1-1 modulators is not completely uncorrelated, although it remains largely independent.

Additional quantization noise at low frequencies can arise from the interaction between quantization noise and circuit nonlinearities, sometimes referred to as nonlinearity-

induced stochastic noise. As can be seen at low frequencies in Figure 5.16, this noise is also suppressed by the linearization scheme.

The ENOP SDM in [48] is immune to spurs in the presence of second- and third-order nonlinearities. In terms of spur performance, it clearly surpasses the approach in which MASH 1-1 modulators are operated with time offsets, where spurs cannot be fully suppressed. However, the ENOP SDM introduces a larger time error at the input of the phase detector, leading to increased quantization noise. This tradeoff warrants a comparison between the discussed linearization scheme and the ENOP SDM.

The same closed-loop setup used in the simulations of the MASH 1-1 with and without offset in Figure 5.16 is employed here as well, with the only difference being that the fractional control word is set to 0.00039. The simulation results are shown in Figure 5.17, where the red curve belongs to the ENOP SDM and the blue curve corresponds to two MASH 1-1 modulators driven with a time offset of 0.5, as in the setup of Figure 5.16. As evident from Figure 5.17, the MASH 1-1 exhibits a spur at twice the fractional frequency, whereas the ENOP SDM does not produce spurs.

However, the total quantization noise integrated from 10 kHz to 100 MHz for the MASH 1-1 is only 3.7 ps, including the power of the spur, while the ENOP SDM exhibits a quantization noise of 8.7 ps. The substantially higher noise floor of the ENOP at lower frequencies can be attributed to the large time error it produces at the input of the phase detector, thereby effectively experiencing a stronger nonlinearity.

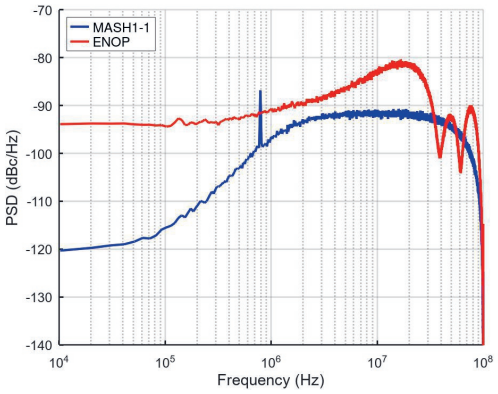


Figure 5.17: Red curve: PSD from quantization noise of ENOP SDM. Blue curve: PSD form two SDM with half a period offset.

5.5.5 Efficient Hardware Implementation

The implementation shown in Figure 5.9. requires two SDMs, two frequency dividers, and two phase detectors. Each individual phase detector can be scaled down

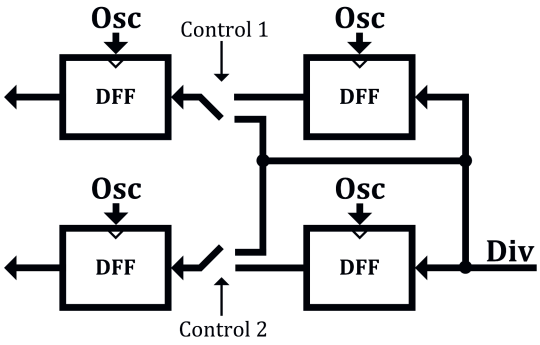


Figure 5.18: Efficient hardware implementation of the proposed linearization scheme.

to half the size compared to a single phase detector system, as the total noise from the phase detector part and the PLL transfer function then remain equivalent. Therefore, with this approach, the phase detector does not introduce significant area or power consumption overhead. The SDMs are implemented digitally and typically occupy very limited silicon area. In modern technologies, their power consumption is negligible [65]. The frequency divider, on the other hand, can consume approximately 0.5 to 1 milliwatt depending on the input frequency [65], [64]. In conclusion, the additional frequency divider represents the most significant drawback in the implementation shown in Figure 5.9. However, the configuration can be simplified as illustrated in Figure 5.18 which eliminates the need for two separate dividers. The implementation in Figure 5.18 is sufficient because both dividers in the original implementation have equivalent input and output frequencies, and the instantaneous time error between them is an integer multiple of the VCO period. The exact same output sequence can be generated by the circuit implementation shown in Figure 5.18. In this configuration, the input and output frequencies remain identical, as the system is driven by a single divider. An arbitrary time error, whose magnitude is constrained to an integer multiple of the VCO period, can be introduced by independently controlling switches Control 1 and Control 2 in Figure 5.18. By appropriately toggling these control switches, the time error can be shifted forward or backward by one VCO period. Hence, the implementation in Figure 5.18 can reproduce the same output as the two divider configuration while requiring only two additional delay flip flops compared to a single SDM-PLL. These flip flops are small, and the larger flip flops used to resynchronize with the oscillator signals can, like the phase detector be scaled down to half size to maintain the same noise, contribution with extra minimum, area and power overhead. Although Figure 5.18, illustrates two output paths, the scheme can be easily extended to include more phase detectors and modulators to suppress additional fractional spur harmonics.

5.6 Proposed PLL with Pseudo differential DTC

Figure 5.19, shows the proposed PLL architecture. The PLL employs a sampling phase detector (SPD) and a two-path VCO, consisting of proportional and integral control paths. similar to [5]. A conventional phase-frequency detector (PFD) and charge pump (CP) are included to provide reliable frequency acquisition and locking. To reduce power consumption, the PFD/CP path is disabled during normal operation. A unity-gain buffer is used to override the SPD when the acquisition path is enabled. Quantization-noise-induced timing errors are mitigated using a pseudo-differential DTC. The divider supports triggering on both rising and falling clock edges, which reduces the timing error of the second-order MASH modulator from two VCO periods to one VCO period. The phase error is extracted by a dedicated extraction circuit and used for least mean square (LMS) based DTC calibration. The calibration compensates both the DTC gain error and the offset arising from mismatch between divider sampling on the positive and negative clock edges.

5.6.1 Phase domain PLL model

The PLL is modeled in the phase domain using the transfer functions of the VCO, divider, and sampling phase detector (SPD). The VCO consists of an integral and a proportional tuning path, resulting in

$$H_{\mathrm{VCO}}(s) = H_{\mathrm{VCO},I}(s) + H_{\mathrm{VCO},P}(s) = \frac{2\pi K_{\mathrm{VCO},I} g_m}{C_I s^2} + \frac{2\pi K_{\mathrm{VCO},P}}{s}. \tag{5.45}$$

The divider transfer function is modeled as

$$H_{\mathrm{div}}(s) = \frac{1}{N} e^{-sT_{\mathrm{div}}}, \tag{5.46}$$

where N is the divider ratio and T_{div} is the divider delay. The SPD transfer function is given by (5.47) and will be explained in the section on the SPD. Equation (5.66) will also motivate the model presented in the SPD section.

$$H_{\mathrm{SPD}}(s) = K_{\mathrm{SPD}} \frac{\lambda e^{-sT_{\mathrm{ref}}/2}}{1-(1-\lambda)e^{-sT_{\mathrm{ref}}}} \frac{1}{T_{\mathrm{ref}} s} \left(1 - e^{-sT_{\mathrm{ref}}}\right). \tag{5.47}$$

$$H_{\mathrm{SPD}}(s) \approx K_{\mathrm{SPD}} \frac{1}{1 + s/\omega_{\mathrm{SPD}}}, \tag{5.48}$$

Using these block transfer functions, the transfer function from the reference input to the PLL output is

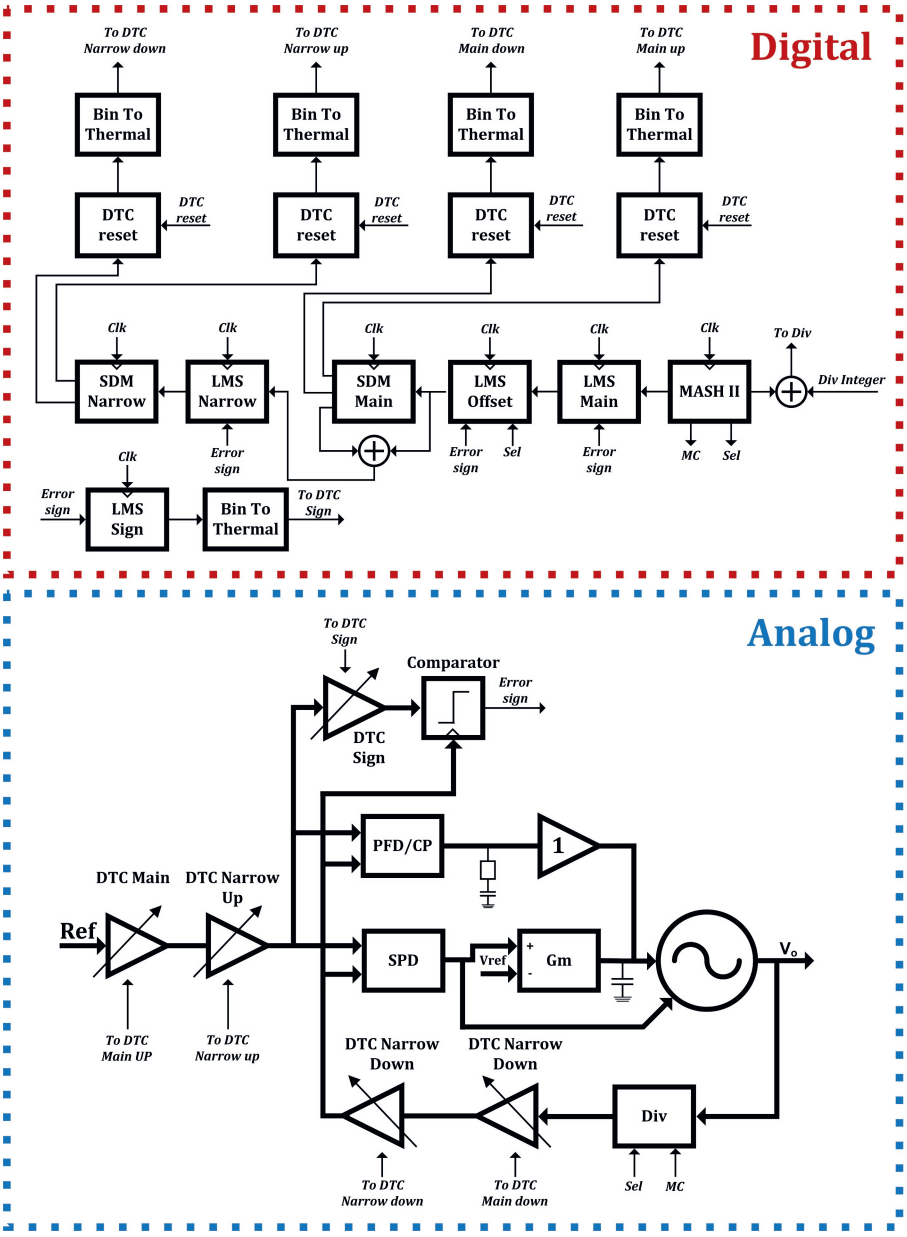


Figure 5.19: Block diagram of the phase-locked loop architecture.

$$H_{\text{ref}\to\text{out}}(s) = \frac{H_{\text{SPD}}(s)H_{\text{VCO}}(s)}{1 + H_{\text{SPD}}(s)H_{\text{VCO}}(s)H_{\text{div}}(s)}. \tag{5.49}$$

Similarly, the transfer function from the VCO phase noise to the PLL output is

$$H_{\text{VCO}\to\text{out}}(s) = \frac{1}{1 + H_{\text{SPD}}(s)H_{\text{VCO}}(s)H_{\text{div}}(s)}. \tag{5.50}$$

Assuming that the divider delay is negligible, the divider transfer function can be approximated as

$$H_{\text{div}}(s) = \frac{1}{N}.$$

Using

$$H_{\text{SPD}}(s) = \frac{K_{\text{SPD}}}{1 + s/\omega_{\text{SPD}}},$$

and the explicit reference-to-output transfer function becomes

$$H_{\text{ref}\to\text{out}}(s) = \frac{\frac{K_{\text{SPD}}}{1+s/\omega_{\text{SPD}}}\left(\frac{2\pi K_{\text{VCO},I} g_m}{C_I s^2} + \frac{2\pi K_{\text{VCO},P}}{s}\right)}{1 + \frac{1}{N}\frac{K_{\text{SPD}}}{1+s/\omega_{\text{SPD}}}\left(\frac{2\pi K_{\text{VCO},I} g_m}{C_I s^2} + \frac{2\pi K_{\text{VCO},P}}{s}\right)}. \tag{5.51}$$

The transfer function in (5.51) contains three poles. Although this expression accurately captures the effect of the SPD pole, its complexity makes it difficult to extract clear design insight. Therefore, in order to simplify the analysis and obtain a more intuitive closed-form expression, the following approximation is introduced.

$$H_{\text{SPD}}(s) = \frac{K_{\text{SPD}}}{1 + \frac{s}{\omega_{\text{SPD}}}} \approx K_{\text{SPD}}, \qquad \omega_{\text{SPD}} \gg \omega_{\text{BW}}. \tag{5.52}$$

The approximation is discussed in detail in the section on sampling phase detector.

Using this approximation, (5.51) can be written as (5.53), and further rearranged into the standard second-order form in (5.55). The natural frequency ω_n is approximately equal to the PLL bandwidth, as given in (5.59) [12]. The damping factor ζ is typically chosen to be around unity in order to obtain good stability and limited transfer-function peaking. Equations (5.56) and (5.57) therefore provide a useful starting point for the PLL design.

However, since the results depend on the approximations transfer function, the full transfer function should be used. Validation should be performed by comparing the full MATLAB model with schematic-level simulations.

$$H_{\text{ref}\to\text{out}}(s) = \frac{K_{\text{SPD}}\left(\frac{K_I}{s^2} + \frac{K_P}{s}\right)}{1 + \frac{K_{\text{SPD}}}{N}\left(\frac{K_I}{s^2} + \frac{K_P}{s}\right)}. \tag{5.53}$$

$$H_{\text{ref}\to\text{out}}(s) = \frac{K_{\text{SPD}}\left(K_P s + K_I\right)}{s^2 + \frac{K_{\text{SPD}}K_P}{N}s + \frac{K_{\text{SPD}}K_I}{N}}. \tag{5.54}$$

$$H_{\text{ref}\to\text{out}}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{5.55}$$

$$\omega_n = \sqrt{\frac{K_{\text{SPD}}K_I}{N}}. \tag{5.56}$$

$$\zeta = \frac{K_{\text{SPD}}K_P}{2N\omega_n}. \tag{5.57}$$

$$K_I = \frac{2\pi K_{\text{VCO},I} g_m}{C_I}, \qquad K_P = 2\pi K_{\text{VCO},P}. \tag{5.58}$$

$$0.1\omega_{\text{BW}} \approx 2.5\omega_n. \tag{5.59}$$

Figure 5.20 shows the complete MATLAB-simulated transfer functions for the PLL building blocks, together with the corresponding noise contributions indicated in the top-right corner of the plot. The parameters used in the simulation are summarized below: $N = 80$, $T_{\text{ref}} = 10\,\text{ns}$, $C_{s1} = C_{s2} = 0.75\,\text{pF}$, $\lambda = C_{s1}/(C_{s1} + C_{s2}) = 0.5$, $K_{\text{VCO},I} = 200\,\text{MHz/V}$, $K_{\text{VCO},P} = 20\,\text{MHz/V}$, $g_m = 20\,\mu\text{S}$, and $C_I = 40\,\text{pF}$.

5.6.2 Sampling Phase Detector

Figure 5.21 shows the schematic of the sampling phase detector (SPD). When the reference signal transitions low, the PMOS device turns on and charges capacitor C_1, while the NMOS device is turned off. When the feedback signal fb from the divider subsequently arrives, the first sampling switch samples the charge on capacitor C_1. The complementary signal $\overline{\text{fb}}$ opens the second switch, and charge sharing between C_1 and C_2 occurs.

The switched-capacitor SPD can first be described in the z-domain. The charge sharing between C_1 and C_2 gives the recursive relation in eq (5.60).

$$v_{\text{out}}[n] = \lambda v_{\text{in}}\left[n - \frac{1}{2}\right] + (1-\lambda)v_{\text{out}}[n-1], \tag{5.60}$$

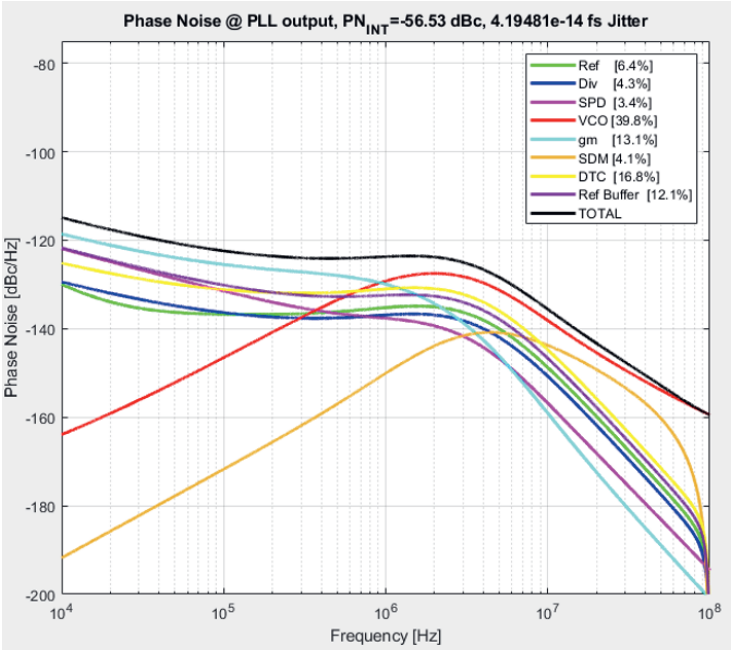


Figure 5.20: PLL phase noise contribution.

where the charge-sharing factor is given by

$$\lambda = \frac{C_1}{C_1 + C_2}. \tag{5.61}$$

Taking the z-transform of (5.60), the switched-capacitor transfer function becomes

$$H_{\mathrm{SC}}(z) = \frac{V_{\mathrm{out}}(z)}{V_{\mathrm{in}}(z)} = \frac{\lambda z^{-1/2}}{1 - (1-\lambda)z^{-1}}. \tag{5.62}$$

The zero-order hold effect over one reference period is modeled as

$$H_{\mathrm{ZOH}}(s) = \frac{1 - e^{-sT_{\mathrm{ref}}}}{sT_{\mathrm{ref}}}. \tag{5.63}$$

Using the mapping

$$z^{-1} = e^{-sT_{\mathrm{ref}}}, \tag{5.64}$$

The full SPD transfer function is obtained by multiplying the switched-capacitor transfer function with the zero-order hold transfer function and given in eq (5.65).

$$H_{\mathrm{SPD}}(s) = K_{\mathrm{SPD}} \frac{\lambda e^{-sT_{\mathrm{ref}}/2}}{1-(1-\lambda)e^{-sT_{\mathrm{ref}}}} \frac{1-e^{-sT_{\mathrm{ref}}}}{sT_{\mathrm{ref}}}. \tag{5.65}$$

Applying a first-order Taylor expansion to the SPD transfer function yields a first-order approximation with a pole located at

$$H_{\mathrm{SPD}}(s) \approx \frac{K_{\mathrm{SPD}}}{1+\frac{s}{\omega_{\mathrm{SPD}}}}. \tag{5.66}$$

$$\omega_{\mathrm{SPD}} = \frac{C_1}{2\pi C_2}\omega_{\mathrm{ref}}. \tag{5.67}$$

For the common design choice $C_1 = C_2$ and a reference frequency of $f_{\mathrm{ref}} = 100\,\mathrm{MHz}$, the switched-capacitor SPD filter pole is approximately given by (5.68), resulting in $f_{\mathrm{SPD}} \approx 16\,\mathrm{MHz}$. Since this pole frequency is substantially higher than the bandwidth of a typical PLL, the SPD filter has a negligible effect on the loop dynamics within the frequency range of interest. Consequently, the SPD filter can be approximated as an ideal gain element, which simplifies the loop analysis and allows the closed-form expression in (5.53) to be obtained.

$$f_{\mathrm{SPD}} = \frac{\omega_{\mathrm{SPD}}}{2\pi} = \frac{1}{2\pi} f_{\mathrm{ref}} \approx 16\,\mathrm{MHz}. \tag{5.68}$$

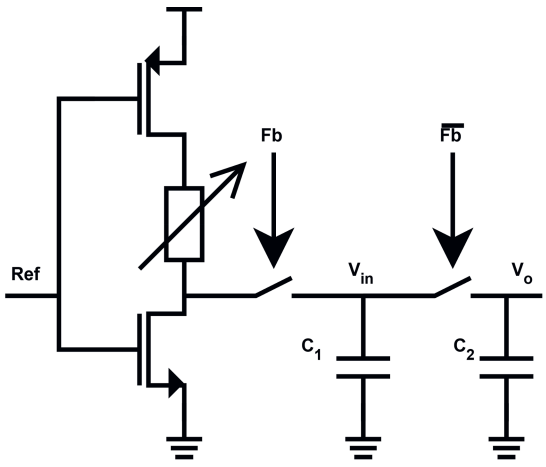


Figure 5.21: Sampling phase detector implementation.

5.6.3 Voltage-Controlled oscillator

The schematic of the oscillator is shown in Fig. 5.22. It is implemented with a tail inductor in order to suppress thermal and flicker noise upconversion from DC to RF [66]. Thick-oxide devices are employed to support a larger voltage swing, thereby improving oscillator robustness and reliability, while allowing the VCO to be biased at 900 mV, consistent with the other building blocks.

A 5-bit binary-coded switched-capacitor bank is added in parallel with the tail coil to provide tunability, since the common-mode impedance can be difficult to predict accurately. The switched-capacitor bank therefore enables tuning of the impedance at the second-harmonic frequency.

In addition, a 4-bit binary-coded tuning block is implemented for frequency setting, and two varactors are employed for the proportional and integral paths, as shown in Fig. 5.22, where the integral path has a tuning coefficient of approximately $K_{\mathrm{VCO},I} =$ 200 MHz/V, while the proportional path has $K_{\mathrm{VCO},P} = 20$ MHz/V. The differential pair transistors are 25um/105nm.

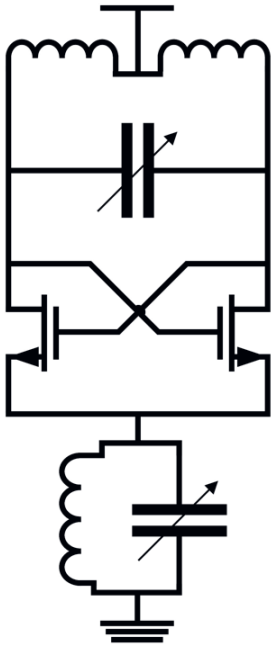


Figure 5.22: Voltage-Controlled Oscillator Implementation.

5.6.4 Proposed Digital-to-Time Converter

The proposed DTC employs a variable-slope architecture due to its superior noise–power tradeoff compared to constant-slope implementations. To achieve high linearity while maintaining low power consumption, the DTC is segmented into coarse and fine stages, each implemented using 6-bit thermometer coding. Furthermore, a pseudo-differential architecture is adopted to suppress even-order nonlinearities, improve supply-noise rejection, and reduce sensitivity to device mismatch.

The nonlinearity of a conventional DTC can be approximated by a polynomial expansion

$$T_{\mathrm{INL}} = a_1 \,\mathrm{code} + a_2 \,\mathrm{code}^2 + a_3 \,\mathrm{code}^3, \tag{5.69}$$

where a_1, a_2, and a_3 represent the linear, second-order, and third-order coefficients, respectively. In a conventional single-ended implementation, the quadratic term contributes directly to the overall integral nonlinearity and can generate significant fractional spurs. and is often the biggest source of nonlinearity in variable slope DTCs [65].

To reduce this effect, the input code is split into two complementary paths around a midpoint code m, such that one path is driven by $m + c$ and the other by $m - c$, where c denotes the differential code excursion. The differential output can then be expressed as

$$\begin{aligned} T_{\mathrm{INL,diff}} = &\Big[a_1(m+c) + a_2(m+c)^2 + a_3(m+c)^3\Big] \\ &- \Big[a_1(m-c) + a_2(m-c)^2 + a_3(m-c)^3\Big]. \end{aligned} \tag{5.70}$$

When the architecture is centered around the midpoint ($m = 0$), the second-order contribution is eliminated and

$$T_{\mathrm{INL,diff}} = 2a_1 c + 2a_3 c^3. \tag{5.71}$$

Thus, the pseudo-differential architecture inherently suppresses the quadratic nonlinearity, which is often one of the dominant contributors to fractional spurs in DTC-assisted fractional-N PLLs.

The complete architecture is shown in Figure 5.23. Separate UP and DOWN DTC paths are employed, allowing the charging and discharging currents to remain approximately constant. This reduces sensitivity to supply-voltage variations and mitigates supply-memory effects. Each path consists of a main 6-bit DTC providing the majority of the timing range and a narrow-range 6-bit DTC providing fine timing adjustment. Since the narrow DTC operates over only a limited delay range, its linearity requirements are significantly relaxed, reducing both INL and DNL.

The outputs of the UP and DOWN paths are combined by the sampled phase detector (SPD), forming a pseudo-differential timing interface. In addition to suppressing even-order distortion, the differential operation improves rejection of common-mode disturbances such as supply and substrate noise. Consequently, the proposed architecture achieves improved linearity, enhanced robustness against mismatch and supply variations, and fast calibration with only modest calibration overhead.

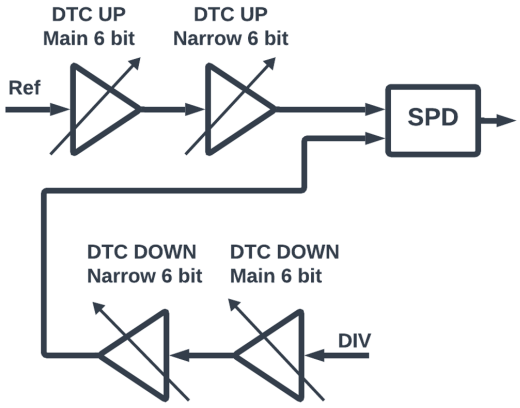


Figure 5.23: DTC architecture implementation.

The schematic-level implementation of both the main and narrow DTCs is shown in Figure 5.24, and the simulated INL of the Main DTC is shown in Figure 5.25. The results clearly show that the even-order INL is eliminated, as predicted by the theory above. Figure 5.26, show the simulated phase noise of one the Main DTCs, for ex DTC up. In Figure 5.24 the resistor is programmable from 75 to 600 ohm and the input transistors are both 100um/30n and the output inverter is 800um/30nm for the PMOS and 400um/30nm for the NMOS.

5.6.5 Freqeuency divider

The divider is commonly implemented as shown in Figure 5.27, where a synchronizing delay flip-flop (DFF) is used to suppress divider phase noise (PN). For robust operation, the divider delay variation across process, voltage, and temperature (PVT) corners must remain below one VCO period. However, this requirement becomes difficult to satisfy at high frequencies and large division. Existing solutions have addressed this issue by calibrating a digital-to-time converter (DTC) to ensure that the divider delay variation remains within one VCO cycle. However, these methods increase circuit complexity and require additional overhead. In this work, the approach shown in Figure 5.27 is adopted instead. Several inverters are inserted before the first synchronizing DFF to introduce a delay tau. Although the inverter chain provides the required delay, it also contributes additional noise. To suppress this

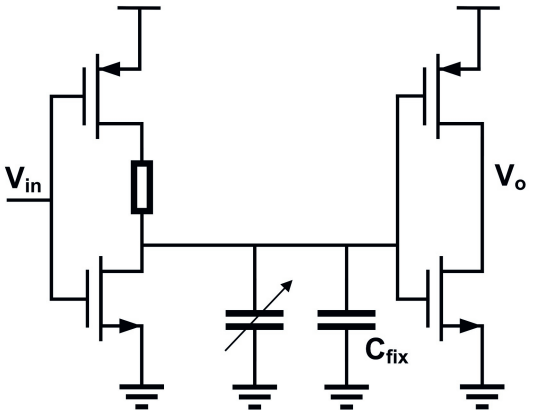


Figure 5.24: DTC schematic implementation.

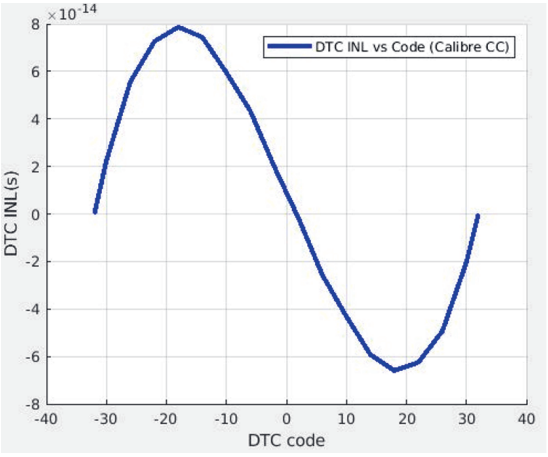


Figure 5.25: INL of Main DTC.

noise, an additional DFF can be inserted, as shown in Figure 5.27(b), such that the inverter-induced noise is attenuated by the subsequent synchronization stage. This can be viewed as using two DFFs to increase the timing margin of the divider. If the divider delay variation is smaller than half a VCO period, the divider timing becomes effectively fixed, thereby improving robustness. The divider itself is implemented as a Cicero divider [67].

5.6.6 Phase Sign Extraction Circuit

An overview of the various existing sign-extraction circuits is shown in Figure 5.28. In Figure 5.28(a), first presented in [65], the phase-error sign is extracted using a com-

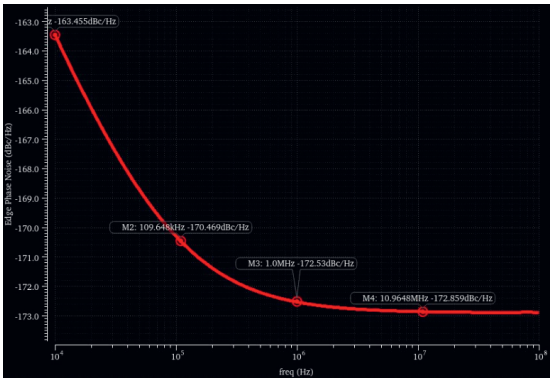


Figure 5.26: Phase noise of Main DTC (simulated).

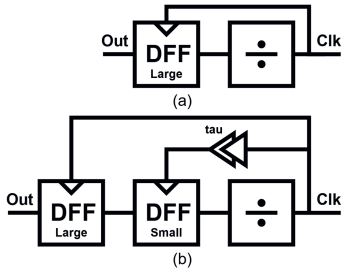


Figure 5.27: Resynchronization topologies. (a) Standard resynchronization circuit. (b) Proposed resynchronization circuit.

parator placed after the sampling phase detector. A single-bit accumulation sigma-delta DAC is used to cancel the voltage offset. However, the main limitation of this approach is the tradeoff between settling speed and offset-cancellation accuracy, which is set by the step size of the accumulation sigma-delta DAC. This issue becomes even more severe in PLLs that support modulation, such as linear frequency chirps, where the sigma-delta DAC must continuously track variations in Vtune [68]. The sign-extraction circuit presented in Figure 5.28(b) [64] directly addresses this issues by extracting the phase-error sign before the phase detector. A DTC is placed in the reference path to compensate for the phase-detector offset. This approach is highly effective when the offset is limited to a few picoseconds. In this case, the DTC time step can be made small, allowing accurate offset compensation and enabling fast, precise calibration. Moreover, the DTC can be implemented efficiently, since strict linearity is not required as long as its transfer function remains monotonic. However, this approach has two main drawbacks. First, it introduces more overhead than an

accumulation sigma-delta DAC, since the DTC may require thermometer coding to guarantee monotonicity, resulting in larger circuit overhead and additional routing for the required control wires. Second, while the approach is effective when the phase-detector offset is limited to a few picoseconds, it becomes less attractive for larger offsets. In some cases, the offset between the reference path and the feedback path can be relatively large and sensitive to supply voltage, process corners, temperature, and operating conditions. This is the case, for example, for the SPD in Figure 5.21, where the offset can be in the range of tens of picoseconds. Moreover, this offset is strongly affected by the gain setting applied through the sampling phase-detector resistor, as well as by PVT variations. These variations can exceed 50 ps, requiring the DTC to cover a larger range and leading to longer calibration time. In some cases, a larger minimum DTC time step may also be required, which degrades the achievable calibration accuracy. The proposed phase-error extraction circuit is shown in Figure 5.29. A replica of the sampling phase detector is used so that variations in supply voltage or gain setting, for example due to changes in the resistor value, are largely cancelled by the replica. The remaining error, which is much smaller and mainly due to mismatch, is compensated by tuning capacitor C1 using a digital feedback loop.

5.6.7 Measurements

The fractional-N PLL is implemented in 28 nm CMOS technology. Figure 5.30 shows the die photograph and the measurement setup is shown in Figure 5.31.

The fabricated chip is tested through wire bonding. The reference signal is provided by a Crystek CVSS-945 crystal oscillator. The reference spur and fractional spur are measured using a R&S FSW spectrum analyzer, while the phase noise is measured using an Keysight SSA-X E5055A phase-noise analyzer. The PCB supply regulation is implemented using a Linear Technology LT3088 low-dropout regulator (LDO). The total power consumption is 8.7 mW from a 900 mV supply. The VCO consumes 3.7 mW, the DTC 2.7 mW, the divider 2 mW, the digital blocks 1 mW, the SPD and g_m stage 0.13 mW, and the sign extractor 0.2 mW.

The measured fractional-N performance is relatively poor, which is likely caused by the fine and coarse DTC supply rails being connected together, resulting in substantial supply crosstalk. For a fractional control word corresponding to a frequency close to an integer channel, the measured integrated jitter is 400 fs and the fractional spur is -40 dBc. For a frequency control word corresponding to a frequency setting farther away from the integer channel, the integrated jitter improves to 300 fs and the fractional spur is reduced to -60 dBc. The measured integer spur is -61 dBc.

Figure 5.32 shows the measured phase noise in integer-N mode in black and the simulated phase noise in red. The measured phase noise is clearly elevated at lower frequency offsets. To identify the source of this discrepancy, a sensitivity analysis was performed on several circuit blocks to determine the origin of the excess noise. It was found that the reference-buffer supply is highly sensitive to supply noise, and that the LDO in this supply path contributes significant additional noise.

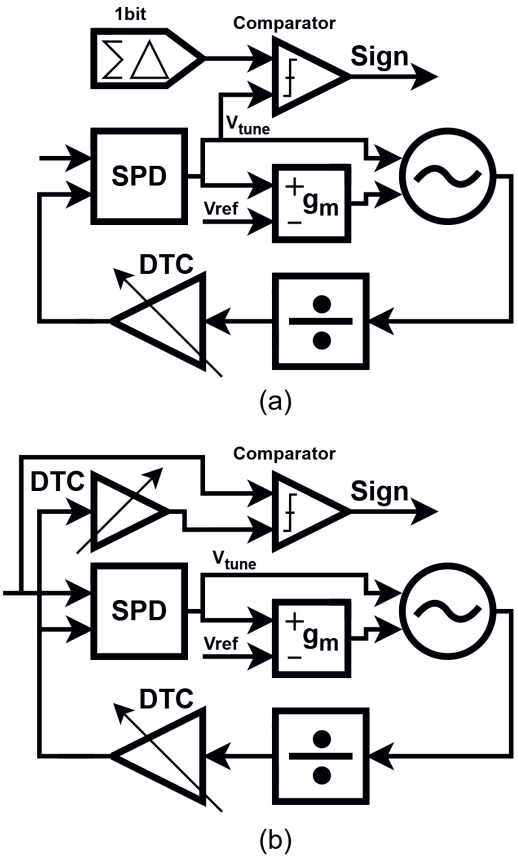


Figure 5.28: Possible topologies for phase error sign extraction. (a) Using a accumulating sigma-delta DAC. (b) Using a DTC and a 1-b TDC.

The contribution from the LDO was estimated by first determining the cutoff frequency of the LDO supply network and subsequently simulating the supply sensitivity of the reference buffer. A small DC variation was applied to the reference-buffer supply, and the resulting timing variation was measured in simulation. By dividing the simulated timing variation by the applied voltage variation, the sensitivity constant could be calculated as

$$K_{\mathrm{VDD},t} = \frac{dt}{dv}.$$

The LDO output noise was extracted from the datasheet, and the resulting phase-noise contribution from the LDO was estimated using (5.72).

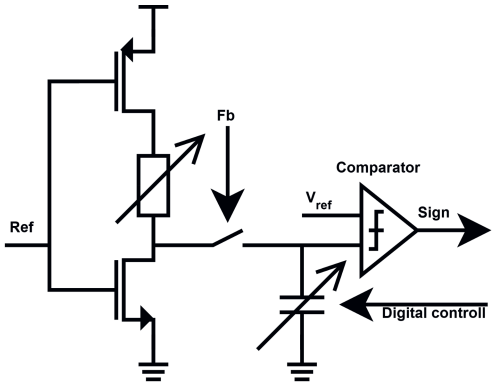


Figure 5.29: Proposed phase error sign extraction circuit.

Table 5.1: State-of-the-Art PLL Comparison Table

	This Work	**JSSC'22 [69]**	**TCAS-I'22 [70]**
Process (nm)	28	40	65
Ref. Freq (MHz)	100	100	100
RMS jitter (fs)	80/42*	48	39
Ref spur (dBc)	−61	−77	−70
FOM (dB)	−253/ − 258*	−259	−258
P_{dc} **(mW)**	8.7	5	9.85
FTR (GHz)	7.8–8.9	9.6–12	8.5–9.5
Supply (V)	0.9	1.1/0.6	1/0.7

*Excluding LDO noise contribution.

$$L_{\mathrm{LDO}}(f) = 10\log_{10}\left(\frac{1}{2}S_{\mathrm{LDO}}(f)\omega_{\mathrm{core}}^2 K_{\mathrm{vdd},t}^2\right) \tag{5.72}$$

The estimated phase noise including the LDO contribution is plotted in blue in Figure 5.32. The simulated phase noise including the LDO contribution shows good agreement with the measured results.

As the fractional-N performance is poor compared to the state of the art, the benchmarking is primarily performed for integer-N operation, which remains reasonably competitive despite the PLL being designed for fractional operation. Table 5.1 compares the proposed PLL operating in integer-N mode with other state-of-the-art integer-N PLLs using comparable reference sources.

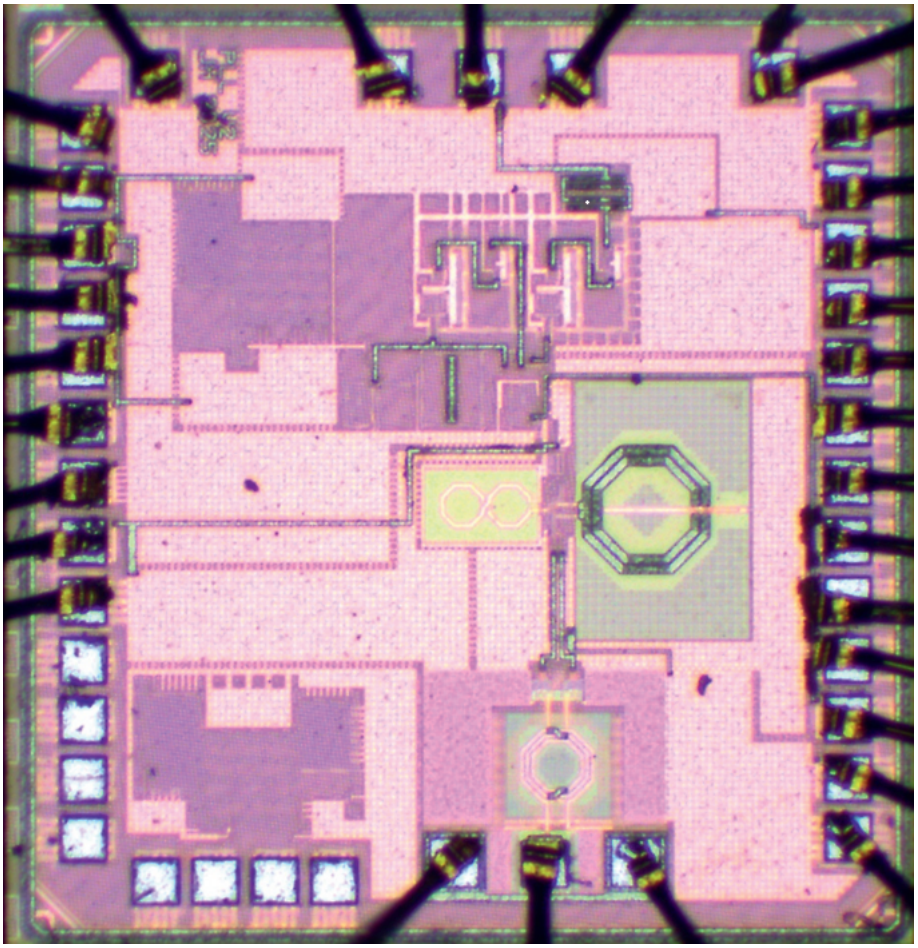


Figure 5.30: Chip photograph.

5.7 Conclusion

This chapter presented the analysis, design, and implementation of a high-performance fractional-N PLL intended for low-jitter and low-spur applications. A comprehensive theoretical framework based on the Periodic Nonlinearity Noise (PNN) theory was used to derive explicit closed-form expressions for fractional spurs originating from second- and third-order nonlinearities. The derived formulas provide valuable design insight by directly relating circuit nonlinearity to fractional-spur magnitude, enabling rapid estimation of spur performance without extensive simulations.

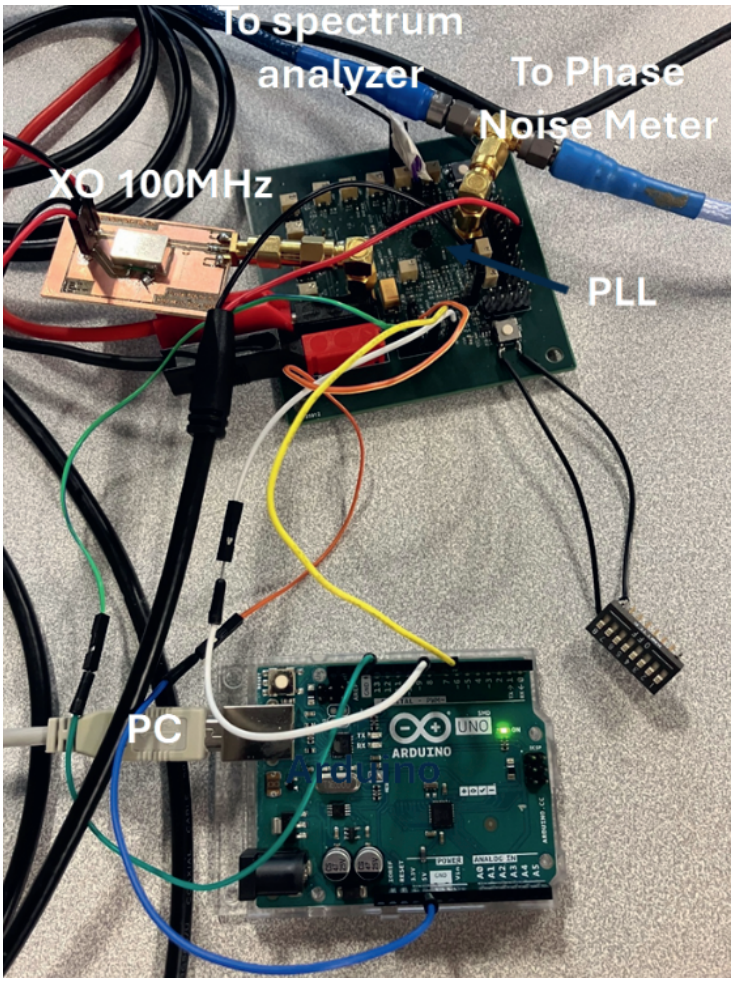


Figure 5.31: Measurement setup.

Building on the PNN framework, the use of multiple phase-shifted sigma–delta modulators operating in parallel was analyzed in detail. It was shown that parallel SDMs can significantly suppress fractional spurs while simultaneously reducing quantization noise. Analytical expressions were derived for both even- and odd-order nonlinearities, and the impact of phase compensation and mismatch mechanisms was investigated. The analysis demonstrated that substantial spur suppression can be achieved with relatively modest hardware overhead, particularly for even-order nonlinearities, while odd-order suppression requires accurate phase alignment. The theoretical predictions were verified through MATLAB simulations and showed good agreement with the

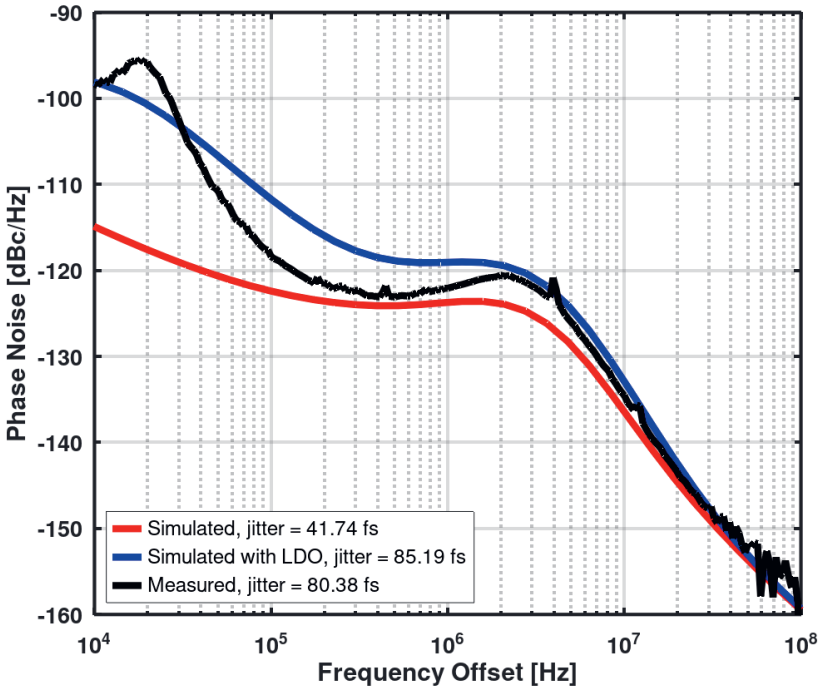


Figure 5.32: Measured phase noise in black, simulated phase noise in red, and simulated phase noise in blue, where the LDO noise is taken from the data sheet.

derived expressions.

A state-of-the-art review highlighted the limitations of existing spur-reduction techniques, including digital predistortion, dithering, cascaded PLLs, and advanced SDM architectures. While many of these approaches achieve excellent spur performance, they often introduce penalties in power consumption, calibration complexity, implementation area, or quantization noise. The parallel-SDM approach analyzed in this work offers an attractive alternative by providing both spur suppression and quantization-noise reduction without significantly increasing the timing-error range at the phase detector input.

To address one of the most critical sources of nonlinearity in fractional-N PLLs, a highly linear pseudo-differential digital-to-time converter (DTC) was proposed. The pseudo-differential architecture improves timing linearity while maintaining an attractive noise-power tradeoff, making it particularly suitable for demanding low-jitter applications. Combined with the proposed PLL architecture, the DTC reduces the

conversion of quantization noise into fractional spurs and enables improved overall spectral purity. Furthermore, a novel phase-extraction circuit was introduced and implemented in a 28 nm bulk CMOS technology together with the proposed PLL building blocks.

Overall, the presented work demonstrates that careful system-level analysis combined with highly linear circuit techniques can substantially improve fractional-N PLL performance. The combination of the pseudo-differential DTC, the parallel-SDM linearization technique, and the derived PNN-based design methodology provides an effective framework for achieving low phase noise, low fractional spurs, and high energy efficiency in next-generation frequency synthesizers.

Chapter 6

Conclusions

This thesis has investigated high-performance frequency synthesizer circuits and local-oscillator (LO) distribution techniques for millimeter-wave communication and radar systems. The work was motivated by the increasing importance of accurate, low-noise, and power-efficient oscillator signal generation in modern transceiver architectures. As carrier frequencies move further into the mmWave and sub-THz range, the requirements on phase noise, output power, frequency multiplication, chirp linearity, and LO distribution become increasingly demanding. These challenges are particularly important for 5G FR2 communication systems, Wi-Fi systems, and high-performance FMCW radar, where the frequency synthesizer often becomes a key limitation for the overall system performance.

At the system level, this work first examined the requirements imposed by mmWave communication systems. The analysis showed that high-order modulation schemes, such as 64-QAM and 256-QAM, impose strict limits on error-vector magnitude and therefore leave only a limited phase-noise and spur budget for the LO generation circuitry. Since the time-jitter requirement becomes more stringent as the carrier frequency increases, the design of low phase-noise PLLs is essential for future FR2 transceivers. This motivates the use of architectures that combine low intrinsic noise with efficient frequency generation and distribution.

The thesis then extended the system-level discussion to FMCW radar systems. Fundamental radar performance metrics such as range resolution, velocity resolution, angular resolution, link budget, and dynamic range were reviewed. Particular attention was given to the potential of D-band radar, where the shorter wavelength and larger available bandwidth can improve both range and angular resolution. However, operation at substantially higher frequencies also introduces important challenges, including increased path loss, reduced output power, degraded phase-noise performance, and more demanding requirements on RF signal generation and distribution. The analysis also emphasized that, in FMCW radar, chirp linearity cannot be fully characterized by a single RMS frequency-error number. Instead, the spectral content of the chirp error must be considered, since different distortion components can

have very different effects on the radar output. This led to an improved methodology for benchmarking chirp linearity with stronger connection to actual radar-system performance.

To address the need for efficient LO generation at high frequencies, a frequency multiplication approach was investigated. A frequency doubler topology was proposed that improves upon conventional push–push doublers by using a fully differential architecture with current reuse. The proposed topology enables higher voltage conversion gain, improved drain efficiency, and a more robust differential-to-differential transformer implementation. By avoiding the limitations associated with single-ended transformer structures and poor balancing, the topology becomes well suited for LO generation in mmWave systems. The implemented 28-nm CMOS frequency upconverter demonstrates the feasibility of this approach and highlights the importance of optimizing frequency multipliers for voltage swing, power consumption, and phase noise when they are used to drive mixers or other high-impedance LO loads.

Finally, the thesis investigated fractional-N PLL architectures and the nonlinearities that limit their spur performance. Closed-form expressions were derived for fractional spurs caused by second- and third-order nonlinearities using the Periodic Nonlinearity Noise framework. These expressions provide useful design insight by directly relating nonlinear time-domain errors to spur levels at the PLL output. The study further showed how multiple sigma–delta modulators operated in parallel with time offsets can suppress fractional spurs and reduce the impact of nonlinearities. In addition, a pseudo-differential digital-to-time converter was proposed to improve linearity by suppressing even-order distortion while also improving supply sensitivity. The implemented fractional-N PLL in 28-nm CMOS demonstrates the relevance of this approach for achieving low phase noise and low spur levels without relying on overly complex calibration.

Overall, the contributions of this thesis show that future mmWave communication and radar systems require a combination of system-level insight and circuit-level innovation. Efficient LO distribution, high-performance frequency multiplication, accurate chirp synthesis, and low-noise fractional-N PLLs must be considered together rather than as isolated circuit blocks. The presented analyses and circuit implementations provide design methods and practical building blocks for next-generation high-frequency transceivers. In particular, the work highlights that improving oscillator signal generation is not only a matter of reducing phase noise, but also of managing nonlinearities, distribution losses, chirp distortions, and power consumption in a complete system context.

6.1 Future Work

A natural continuation of this work is the development of a complete chirp-generating PLL for high-performance FMCW radar systems. Such a design would directly connect the system-level analysis of chirp linearity and radar performance presented in

Chapter 3 with the fractional-N PLL techniques investigated in Chapter 5. In particular, the pseudo-differential DTC architecture, the analysis of fractional spurs, and the use of multiple sigma–delta modulators operated in parallel could be applied to a PLL intended not only for fixed-frequency LO generation, but also for accurate wideband frequency chirp synthesis.

For FMCW radar, the relevant performance metric is not only the integrated phase noise or the RMS chirp error, but also the spectral distribution of the chirp distortion. As discussed in Chapter 3, different frequency-error components can have very different effects on the radar output, even when the total RMS error is identical. Therefore, future PLL design should be optimized using a radar-oriented chirp-linearity metric rather than only conventional PLL metrics such as integrated jitter, phase noise, and fractional-spur level. This would allow the chirp-generation circuit to be evaluated directly in terms of its effect on target detection, dynamic range, and range-profile degradation.

The fractional-N PLL analysis in Chapter 5 provides a useful starting point for such a system. The closed-form expressions for spur generation from nonlinearities can be extended to the case of time-varying fractional frequency control words used during chirp generation. This would make it possible to predict which nonlinearities in the DTC, phase detector, or divider path are most likely to create deterministic chirp distortions. Furthermore, the pseudo-differential DTC can be investigated as a way to improve chirp linearity by suppressing even-order distortion and reducing sensitivity to supply noise. The use of several time-offset sigma–delta modulators in parallel may also be valuable, since it could reduce deterministic spur components that otherwise appear as structured errors in the generated chirp.

Another important direction is to study the interaction between the chirp-generating PLL and the LO distribution architecture in a complete MIMO FMCW radar system. Since phase-noise correlation between the transmitter and receiver paths is essential for suppressing TX-to-RX phase-noise spillover, the chirp generator should be evaluated together with the LO distribution network rather than as an isolated block. This is especially important for mmWave and sub-THz radar systems, where LO distribution loss, frequency multiplication, and phase-noise degradation can strongly affect the final radar dynamic range.

Overall, future work should aim to design, implement, and experimentally verify a chirp-generating fractional-N PLL whose performance is benchmarked using radar-relevant metrics. Such a circuit would represent a direct bridge between the theoretical chirp-linearity analysis, the system-level radar requirements, and the circuit-level PLL techniques developed in this thesis.

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Original contributions

- An improved frequency doubler is proposed by incorporating a PMOS pair into a conventional push–pull full-wave rectified doubler. This modification enhances drain efficiency through current reuse and enables a larger output swing. Importantly, it allows the use of a differential-to-differential transformer with a higher quality factor, thereby avoiding losses caused by poor balancing. The proposed doubler is implemented in 28-nm bulk CMOS to validate the concept.
- A pseudo-differential digital-to-time converter (DTC) is proposed. It improves linearity by suppressing even-order distortions and offers additional benefits such as improved supply sensitivity rejection. Furthermore, high performance can be achieved with simpler digital calibration. An N-fractional PLL is implemented in 28-nm bulk CMOS to demonstrate the proposed approach.
- A theoretical study is conducted on the effects of linearity and quantization noise when multiple sigma–delta modulators operate in parallel with time offsets in an N-fractional PLL. Explicit closed-form expressions for fractional spur suppression are derived and verified through simulations.
- A theoretical investigation of systematic distortions in FMCW radar chirps is presented. The resulting analysis provides new insights and leads to an improved methodology for benchmarking chirp linearity.

List of publications

1. J. Holmstedt and H. Sjöland, "Spur Analysis and Linearity Enhancement in Fractional-N Phase Locked Loops Through Parallel Sigma–Delta Modulators With Time Offsets," *IEEE Open Journal of Circuits and Systems*, vol. 7, pp. 21–32, Jan. 2026.

2. J. Holmstedt and P. T. M. Van Zeijl, "FMCW Radar Chirp Linearity Requirements and Benchmarking Approach," 2025 37th International Conference on Microelectronics (ICM), Cairo, Egypt, 2025.

3. J. Holmstedt, V. Vidojkovic, R. van Dommele, D. Milosevic, *et al.*, "A 36 GHz to 144 GHz Frequency Upconverter Employing a Current Reuse Frequency Doubler with a Differential to Differential Transformer," in *Proc. 31st IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Nov. 2024.

4. J. Holmstedt, R. van Dommele, and V. Vidojkovic, "A Fractional-N Phase-Locked Loop with a Pseudo-Differential DTC and a Phase-Error Sign Extraction Circuit Based on a Phase-Detector Replica," accepted for presentation at the 2026 IEEE 33rd International Conference on Electronics, Circuits and Systems (ICECS), Thessaloniki, Greece, 2026.

5. V. Vidojkovic, D. Milosevic, K. Ding, J. Holmstedt, *et al.*, "RF and mm-Wave Systems and Circuits for Communications and Sensing," 2023 58th International Scientific Conference on Information, Communication and Energy Systems and Technologies (ICEST), Nis, Serbia, 2023.

Summary

Title: High-Performance Frequency Synthesizer Circuits and Local Oscillator Distribution for Radar and Millimeter-Wave Communication Architectures

This work addresses key challenges in oscillator signal generation and distribution for millimeter-wave (mmWave) communication and radar systems. To enable further improvements in overall system performance, several critical issues must be considered. These include the development of power-efficient local oscillator (LO) distribution architectures and ultra-low phase-noise fractional-N phase-locked loops (PLLs) for next-generation FR2 transceivers and Wi-Fi systems. In addition, frequency-modulated continuous-wave (FMCW) radar systems with high dynamic range require highly linear frequency chirps and extremely low phase noise. Furthermore, in FMCW multiple-input multiple-output (MIMO) radar systems, correlation of phase noise between the transmitter (TX) and receiver (RX) is essential to suppress phase-noise spillover from TX to RX. All these aspects must be carefully addressed while maintaining low power consumption.

The work carried out has resulted in the following research contributions:

- An improved frequency doubler is proposed by incorporating a PMOS pair into a conventional push–pull full-wave rectified doubler. This modification enhances drain efficiency through current reuse and enables a larger output swing. Importantly, it allows the use of a differential-to-differential transformer with a higher quality factor, thereby avoiding losses caused by poor balancing. The proposed doubler is implemented in 28-nm bulk CMOS to validate the concept.

- A pseudo-differential digital-to-time converter (DTC) is proposed. It improves linearity by suppressing even-order distortions and offers additional benefits such as improved supply sensitivity rejection. Furthermore, high performance can be achieved with simpler digital calibration. An N-fractional PLL is implemented in 28-nm bulk CMOS to demonstrate the proposed approach.

- A theoretical study is conducted on the effects of linearity and quantization

noise when multiple sigma–delta modulators operate in parallel with time offsets in an N-fractional PLL. Explicit closed-form expressions for fractional spur suppression are derived and verified through simulations.

- A theoretical investigation of systematic distortions in FMCW radar chirps is presented. The resulting analysis provides new insights and leads to an improved methodology for benchmarking chirp linearity.

Biography

Johan Holmstedt received the M.Sc. degree in electrical engineering from Lund University, Sweden, in 2020, and is currently working towards his PhD degree from Eindhoven University of Technology. He worked as an analog design engineer at Ericsson, Lund, Sweden, during 2020. His research interests include design of microwave, mm wave integrated circuits, high performance PLLs and ADCs primarily for radar applications.

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